Troubleshooting – Baseband

Contents

Troubleshooting Overview

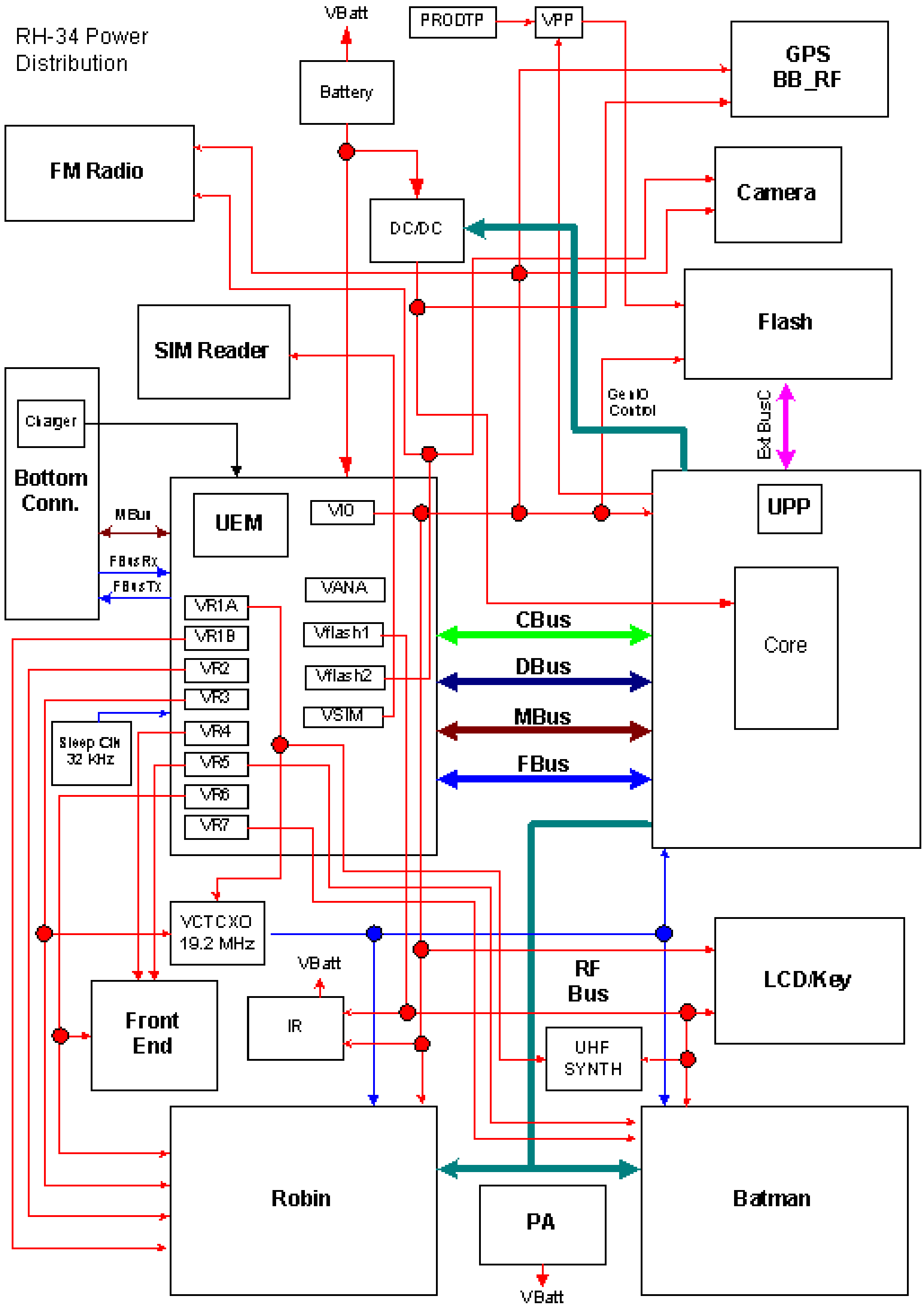
The Baseband module of the RH-34 transceiver is a trimode CDMA dual band engine. The Baseband architecture is based on the DCT4 Apollo engine.

RH-34 Baseband consists of three main ASIC's: Universal Energy Management (UEM), Universal Phone Processor (UPP), and a 128-Megabit FLASH.

The Baseband architecture supports a power-saving function called "sleep mode". This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and Baseband. During the sleep mode, the system runs from a 32 kHz crystal. The phone awakes by a timer running from this 32 kHz clock. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the 19.2MHz Clk (VCTCXO) is switched off.

RH-34 supports both two and three DCT3 type wire chargers. However, the three-wire chargers are treated as two-type wire chargers. Charging is controlled by UEM ASIC and EM SW.

BLD-3 Li-ion battery is used as main power source for RH-34. BLD-3 has nominal capacity of 780 mAh.


RH-34 Power Distribution
VBatt
Battery
PRODTP
VPP
GPS BB_RF
FM Radio
DC/DC
Camera
Flash
SIM Reader
GenIO Control
ExtBusC
Chrger
Bottom Conn.
MBus
FBusRx
FBusTx
UEM
VIO
VANA
VR1A
VR1B
VR2
VR3
VR4
VR5
VR6
VR7
Vflash1
Vflash2
VSIM
Sleep Clk 32 kHz
UPP
Core
CBus
DBus
MBus
FBus
VCTCXO 19.2 MHz
VBatt
IR
RF Bus
UHF SYNTH
LCD/Key
Front End
Robin
PA
Batman
VBatt

Power Up and Reset

Power up and reset is controlled by the UEM ASIC. RH-34 baseband can be powered up in the following ways:

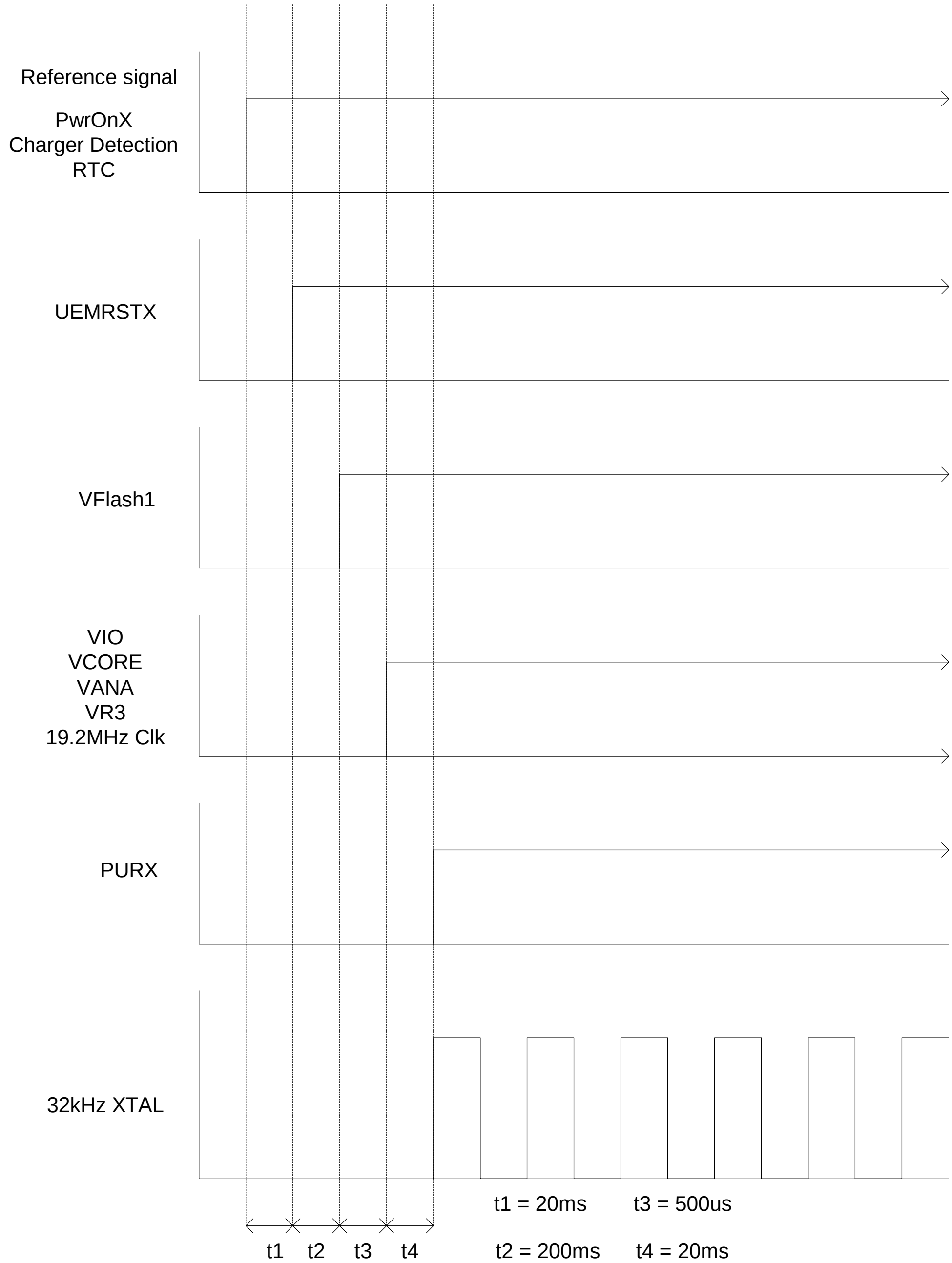
1 By the Power button, which means grounding the PWRONX pin of the UEM

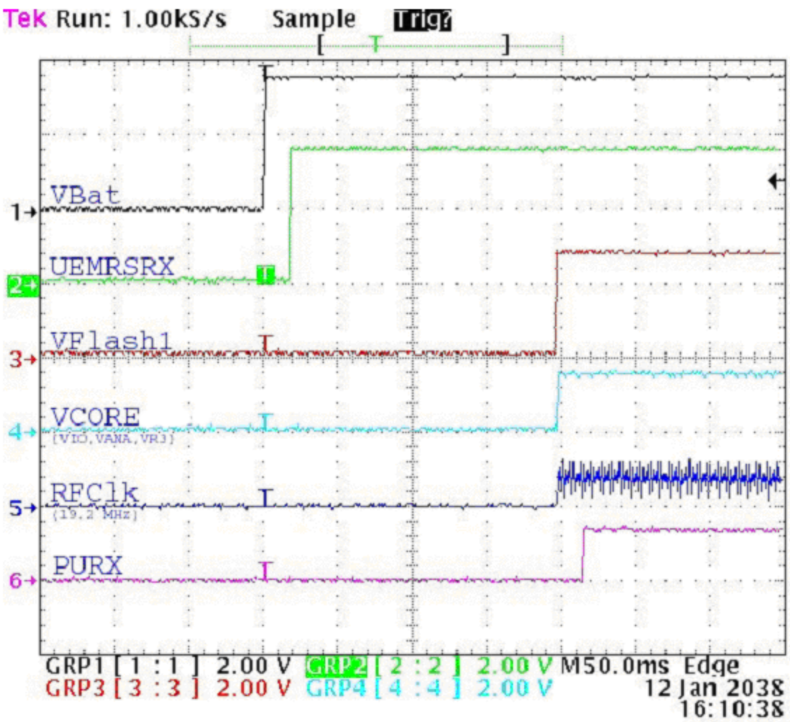
2 By connecting the charger to the charger input

3 By the RTC Alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20ms delay and then enters in reset mode. The watchdog starts up, and if the battery voltage is greater than Vcoff+, a 200ms delay is started to allow references, etc. to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500us later VR3, VANA, VIO, and VCORE are enabled. Finally, the PURX (Power Up Reset) line is held low for 20 ms. This reset, PURX, is fed to the baseband ASIC UPP; resets are generated for the MCU and the DSP. During this reset phase, the UEM forces the VCTCXO regulator on — regardless of the status of the sleep control input signal — to the UEM. The FLSRSTx from the ASIC is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on when the UEM powers on. The UEM internal watchdogs are running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power-off state. The UEM watchdogs are internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

The following diagram represents UEM start-up sequence from reset to power-on mode.


Reference signal
PwrOnX
Charger Detection
RTC
UEMRSTX
VFlash1
VIO
VCORE
VANA
VR3
19.2MHz Clk
PURX
32kHz XTAL
t1 t2 t3 t4
t1 = 20ms
t3 = 500us
t2 = 200ms
t4 = 20ms



Power up with PWR key

When the Power on key is pressed, the UEM enters the power up sequence. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key, an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a certain time, the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power on situation the MCU powers off the baseband.

Power up when charger is connected

In order to be able to detect and start charging in the case where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by START-UP CHARGING circuitry.

Whenever VBAT level is detected to be below master reset threshold (VMSTR-), charging starts and is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above the charger detection threshold, VCHDET+, and by detection charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As battery charges, its voltage rises and when VBAT voltage level is detected to be higher than the master reset threshold limit (VMSTR+), START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). MSTRX='1' output reset signal (internal to UEM) is given to UEM's RESET block when VBAT>VMSTR+ and UEM enters into reset sequence.

If VBAT is detected to fall below VMSTR- during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCHDET+).

RTC alarm power up

If phone is in POWER_OFF mode when RTC alarm occurs, a wake-up procedure occurs. After baseband is powered ON, an interrupt is given to MCU. When RTC alarm occurs during ACTIVE mode, an interrupt to MCU is generated.

Power Off

The Baseband switches into power off mode if any of following statements is true

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Or if Watchdog timer register expires

The Power down procedure is controlled by the UEM.

Power Consumption and Operation Modes

During power off mode, power (VBAT) is supplied to UEM, BUZZER, VIBRA, LED, PA and PA drivers (Tomcat and Hornet). During this mode, the current consumption on this mode is approximately 35uA. This is the UEM leakage current.

In sleep mode, both processors, MCU and DSP, are in stand-by mode. Phone will go to sleep mode only when by both processors made this request. When SLEEPX signal is detected low by the UEM, the phone enters SLEEP mode. VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode and VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during SLEEP mode. When SLEEPX signal is detected high by the UEM, the phone enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection etc.

In sleep mode, the VCTCXO (19.2MHz Clk) is shut down and the 32 kHz sleep clock oscillator is used as reference clock for the baseband.

The average current consumption of the phone can vary depending mainly on SW state like slot cycle 0, 1, or 2 and if the phone is working on IS95 or IS2000 for CDMA; however, on average is about 6 mA in slot cycle 0 on IS95.

In the ACTIVE mode, the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the phone present state such as: burst reception, burst transmission, if DSP is working etc.

In active mode, SW controls the UEM RF regulators: VR1A and VR1B can be enabled or disabled. These regulators work of the UEM charge pump. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8V or 3.3V. VR2 and VR4 -VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during Sleep mode and cannot be control by SW in the same way as the other regulators. VR3 will only turn off if both processors (DSP and MCU) request to be in sleep mode.

CHARGING mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery indicates the battery type/size. The resistor value corresponds to a specific battery type and capacity. This capacity value is related to the battery technology.

The battery voltage, temperature, size and charging current are measured by the UEM, and the EM charging algorithm controls it.

The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off, when the battery voltage has reached 4.2 V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power

In normal operation, the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell. In the case of Lancelot, the battery capacity is 850 mAh.

The UEM ASIC controls the power distribution to whole phone through the BB and RF regulators excluding the power amplifier (PA) and the DC/DC, which have a continuous power rail directly from the battery. The battery feeds power directly to following parts of the system: UEM, PA, DC/DC, buzzer, Vibra, display- and keyboard lights.

The heart of the power distribution to the phone is the power control ASIC, called UEM. It includes all the voltage regulators and feeds power to the whole system. UEM handles hardware functions of power up so that regulators are not powered and power up reset (PURX) is not released if the battery voltage is less than 2.8 V.

RH-34 Baseband is powered from five different UEM regulators: VANA, VIO, VFLASH1, VFLASH2, and VCORE DC/DC. See Table 1.

UEM voltage regulators: VR1A, VR1B, VR2, VR3, VR4, VR5, VR6 and VR7 are used by RF. See Table 2.

Table 1: RH-34 Baseband Regulators

Regulator	Maximum current (mA)	Vout (V)	Notes
VCORE DD/DC	300	1.5	Output voltage selectable 1.0V/1.3V/1.5V/1.8V Default power at power-up is 1.5V
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (off during sleep and power-off modes)
VSIM	25	3.0	

Table 2: RH-34 RF Regulators

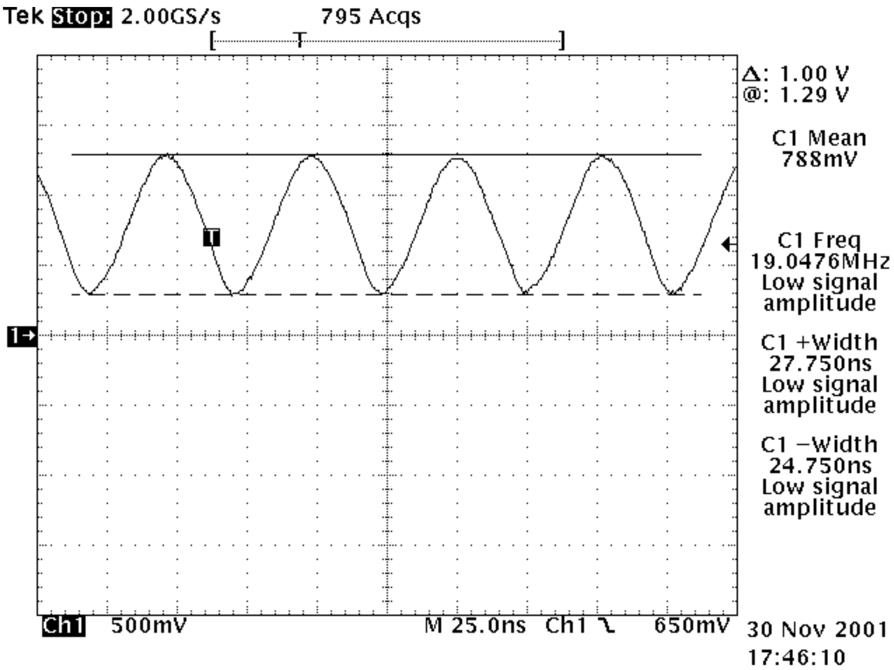
Regulator	Maximum current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when the receiver is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

A charge pump used by VR1A is constructed around UEM. The charge pump works with Cbus (1.2 MHz Clk) and gives a 4.75 V regulated output voltage to RF.

Clock Distribution

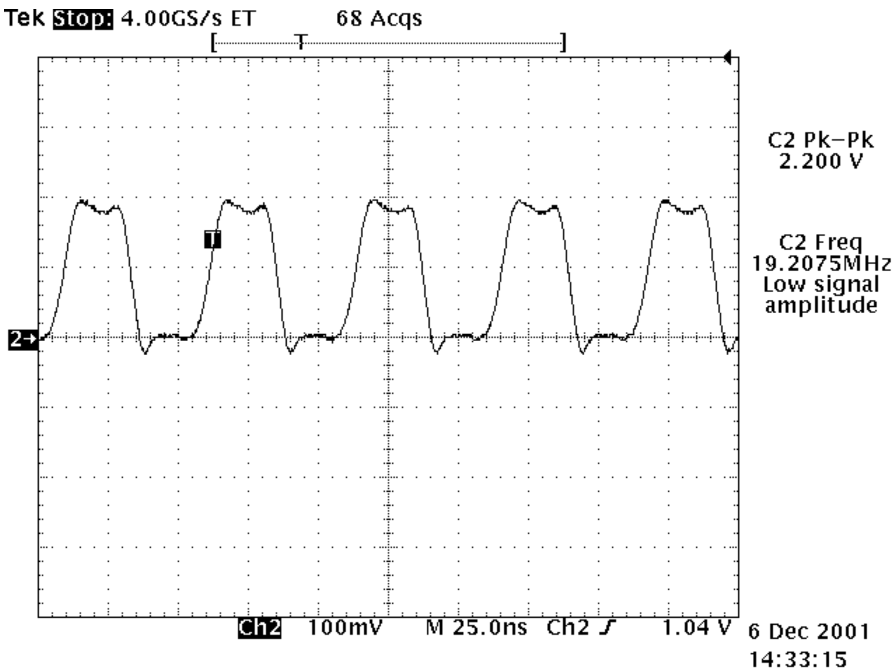
RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator VCTCXO (G503). This 19.2 MHz clock signal is generated at the RF and fed to RFCLK pin of UPP.



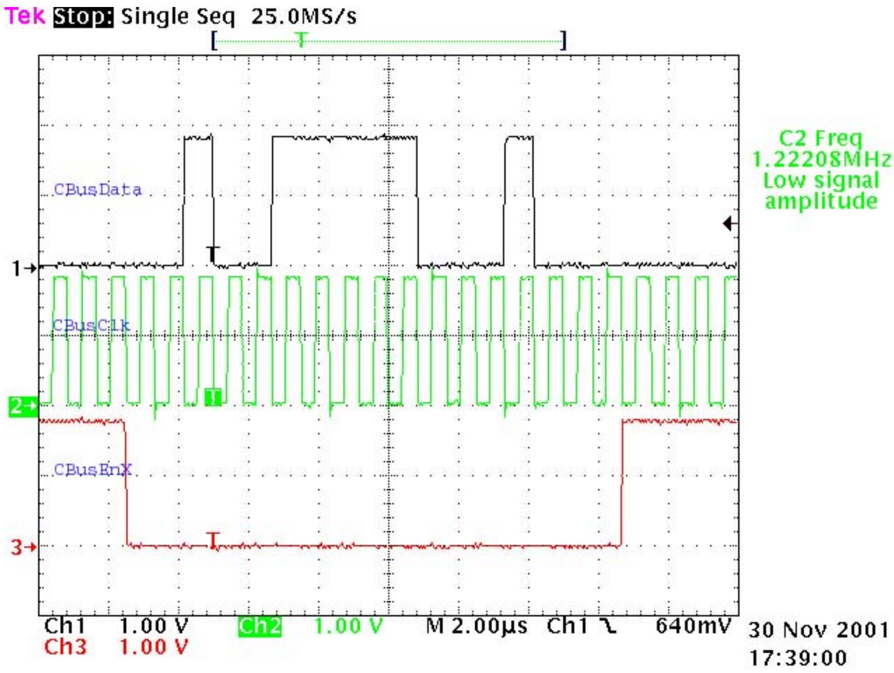
RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2 MHz Clk to the internal processors, the DSP, and MCU, where SW multiplies this clock by seven for the DSP and by two for the MCU.



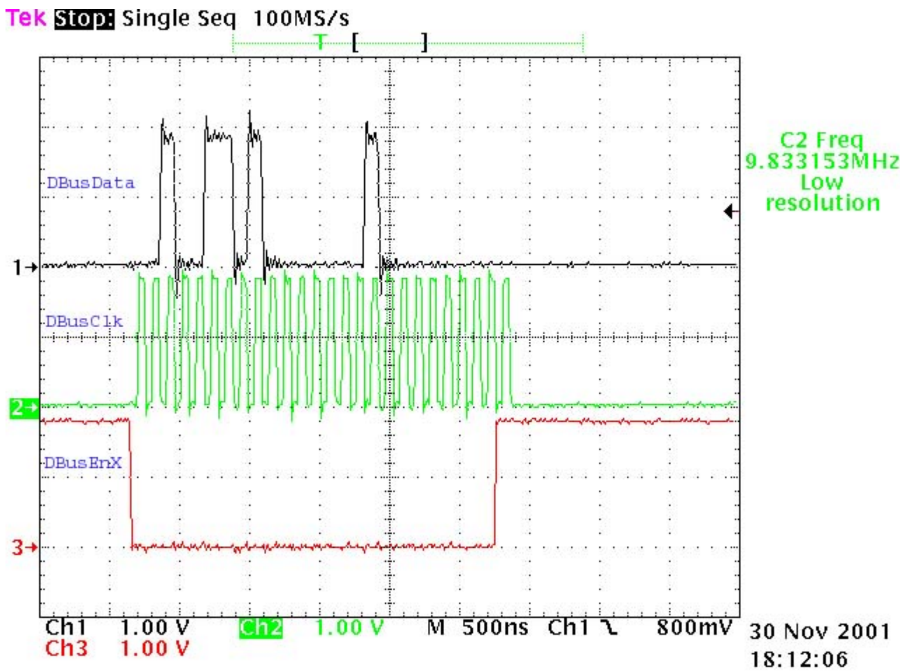
CBUSClk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between UEM and UPP.



DBUS Clk Interface

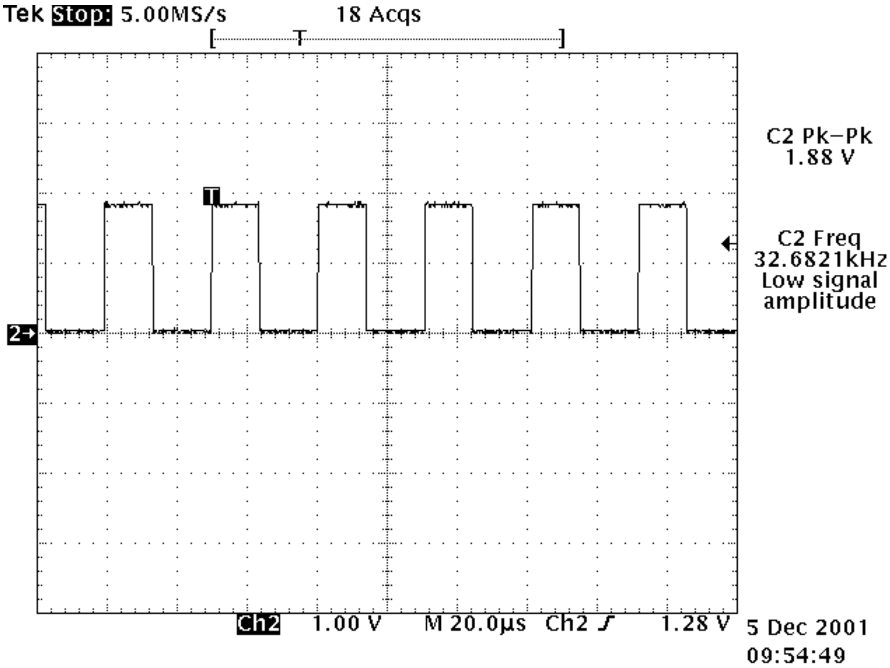
A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between UEM and UPP.



The system clock can stopped during sleep mode by disabling the VCTCXO power supply from the UEM regulator output (VR3) by turning off the controlled output signal SleepX from UPP.

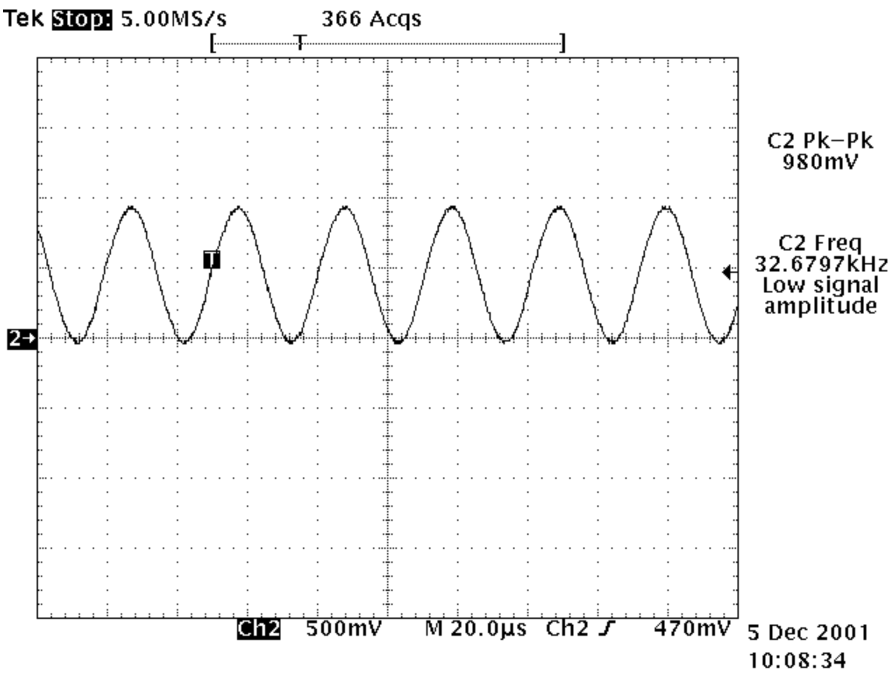
SleepCLK (Digital)

The UEM provides a 32kHz sleep clock for internal use and to UPP, where it is used for the sleep mode timing.



SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32KHz crystal provides a reference to the UEM RTC circuit to turn on the phone during power off or sleep mode.



Flash Programming

Connections to Baseband

The Flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface consist of the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals and use by the FPS8 to flash. The connection is through the UEM which means that the logic voltage levels are corresponding to 2.78V. Power is supplied to the phone using the battery contacts.

Baseband Power Up

The baseband power is controller by the flash prommer in production and in re-programming situations. Applying supply voltage to the battery terminals will cause the baseband to power up. Once the baseband is powered, flash programming indication is done as described in the following section.

Flash Programming Indication

Flash programming is indicated to the UPP using MBUSRX signal between UPP and UEM. The MBUS signal from the baseband to the flash prommer is used as clock for the synchronous communication. The flash prommer keeps the MBUS line low during UPP boot to indicate that the flash prommer is connected. If the UPP MBUSRX signal is low on UPP, the MCU enters flash programming mode. In order to avoid accidental entry to the flash-programming mode, the MCU only waits for a specified time to get input data from the flash prommer. If the timer expires without any data being received, the MCU will continue the boot sequence. The MBUS signal from UEM to the external connection is used as clock during flash programming. This means that flash-programming clock is supplied to UPP on the MBUSRX signal.

The flash prommer indicates the UEM that flash programming/reprogramming by writing an 8-bit password to the UEM. The data is transmitted on the FBUSRX line and the UEM clocks the data on the FBUSRX line into a shift register. When the 8 bits have been shifted in the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content in the UEM into a compare register. If the 8-bits in the compare registers matches with the default value preset in the UEM, programming starts. At this point the flash prommer shall pull the MBUS signal to UEM low in order to indicate to the MCU that the flash prommer is connected. The UEM reset state machine performs a reset to the system, PURX low for 20 ms. The UEM flash programming mode is valid until MCU sets a bit in the UEM register that indicates the end of flash programming. Setting this bit also clears the compare register in the UEM previously loaded at the falling edge of the BSI signal. During the flash programming mode the UEM watchdogs are disabled. Setting the bit indicating end of flash programming enables and resets the UEM watchdog timer to its default value. Clearing the flash programming bit also causes the UEM to generate a reset to the UPP.

The BSI signal is used to load the value into the compare register. In order to avoid spurious loading of the register the BSI signal will be gated during UEM master reset and during power on when PURX is active. The BSI signal should not change state during normal operation unless the battery is extracted, in this case the BSI signal will be pulled high, note a falling edge is required to load the compare register.

Flashing

Flash programming is done through VPP, FBUSTX, FBUSRX, MBUS, and BSI signals.

When phone has entered to flash programming mode, prommer will indicate to UEM that flash programming will take place by writing 8-bit password to UEM. Prommer will first set BSI to "1" and then uses FBUSRX for writing and MBUS for clocking. After that BSI is set back to "0".

MCU will indicate to prommer that it has been noticed, by using FBUSTX signal. After this it reports UPP type ID and is ready to receive secondary boot code to its internal SRAM.

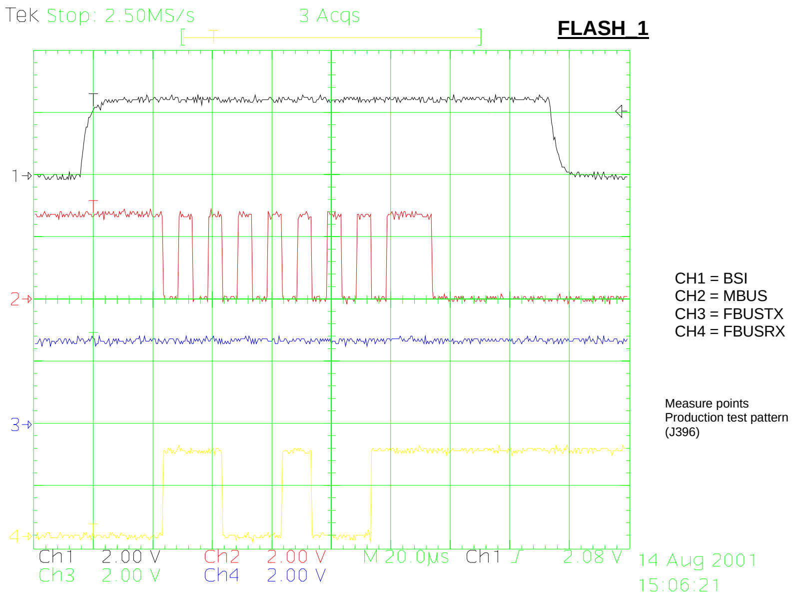


Figure 1: Flashing start

This boot code asks MCU to report prommer phone's configuration information, including flash device type. Now the prommer can select and send algorithm code to MCU SRAM (and SRAM/Flash self-tests can be executed)

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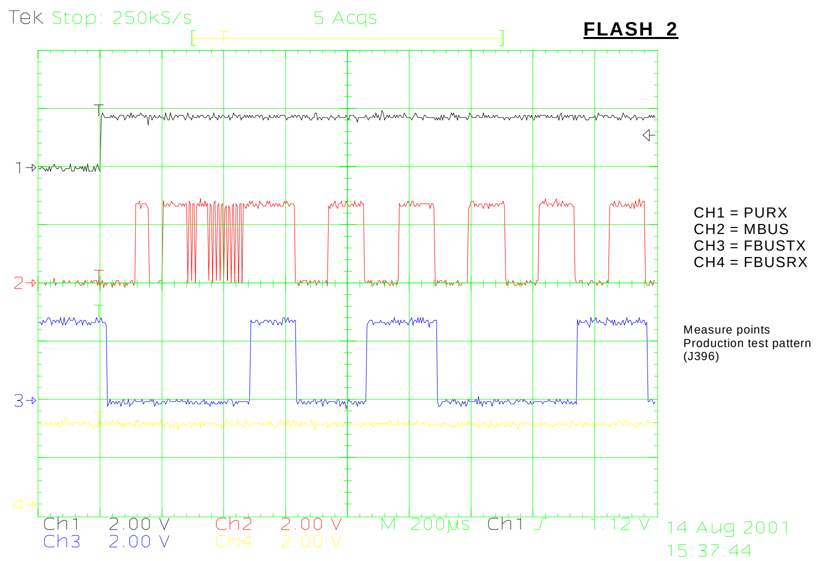


Figure 2: Flashing, continued 1

Ch1-> PURX

Ch2-> MBUS toggled three times for MCU initialization

Ch3-> FBUS_TX low, MCU indicates that prommer has been noticed

Ch4-> FBUS_RX

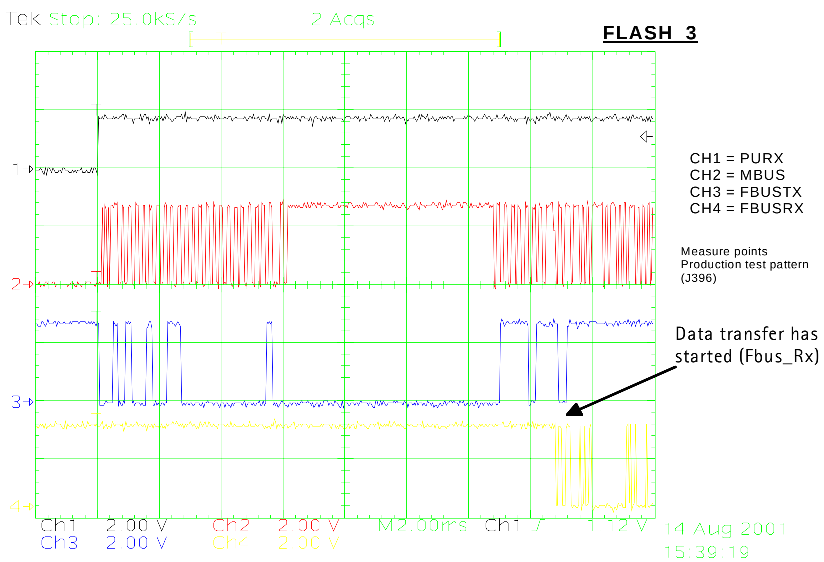


Figure 3: Flashing, continued 2

Charging Operation

Battery

In RH-34, a Lithium-Ion cell battery with a capacity of 780 mAh is used. Reading a resistor inside the battery pack on the BSI line indicates the battery size. NTC-resistor inside the battery measures the battery temperature on the BTEMP line.

Temperature and capacity information are needed for charge control. These resistors are connected to BSI and BTEMP pins of battery connector. Phone has 100 kW pull-up resistors for these lines so that they can be read by A/D inputs in the phone.

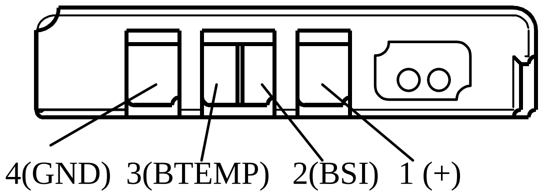


Figure 4: BLB-2 battery pack pin order

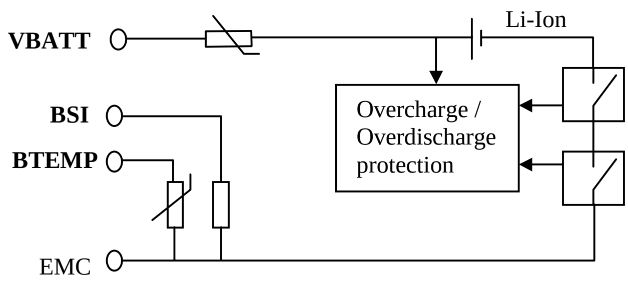


Figure 5: Interconnection diagram inside the battery pack

Charging circuitry

The UEM ASIC controls charging depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The RH-34 baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. However, as mention above, three wire chargers are treated as two.

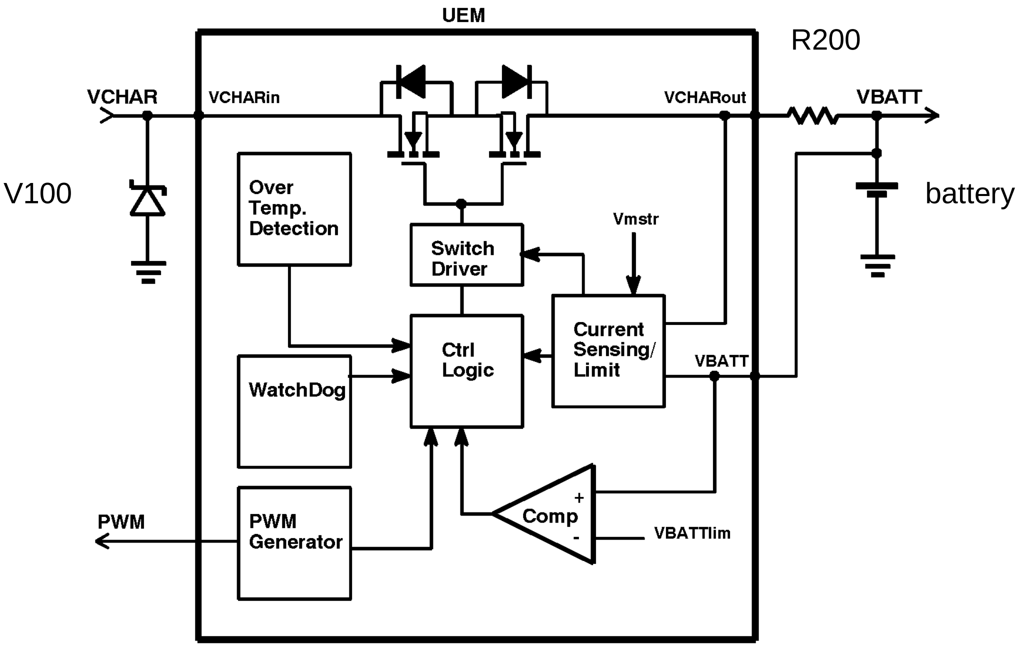


Figure 6: Charging circuitry

Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above 2 V (VCHdet+ threshold) by UEM charging starts. VCHARDET signal is generated to indicate the presence of the charger for the SW. The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

2 Identify the charger as a two-wire or three-wire charger.

3 Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

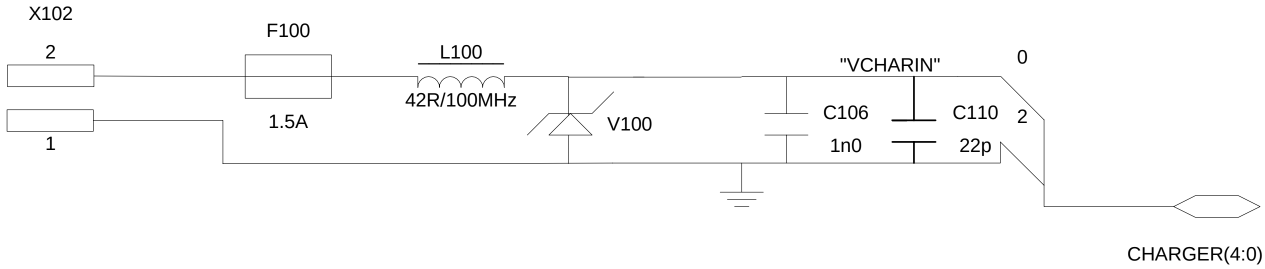


Figure 7: Charging circuit

Charge Control

In active mode, charging is controlled by UEM's digital part. Charging voltage and current monitoring is used to limit charging into safe area. For that reason, UEM has programmable charging cut-off limits:

VBATLim1=3.6 V (Default)

VBATLim2L=5.0 V and

VBATLim2H=5.25 V.

VBATLim1, 2L, 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+ charging is stopped by turning charging switch OFF. No change in operational mode is done. After voltage has decreased below VBATLim- charging re-starts.

There are two PWM frequencies in use depending on the type of the charger: two-wire charger uses a 1Hz and a three-wire charger uses a 32Hz. Duty cycle range is 0% to 100%. Maximum charging current is limited to 1.2 A.

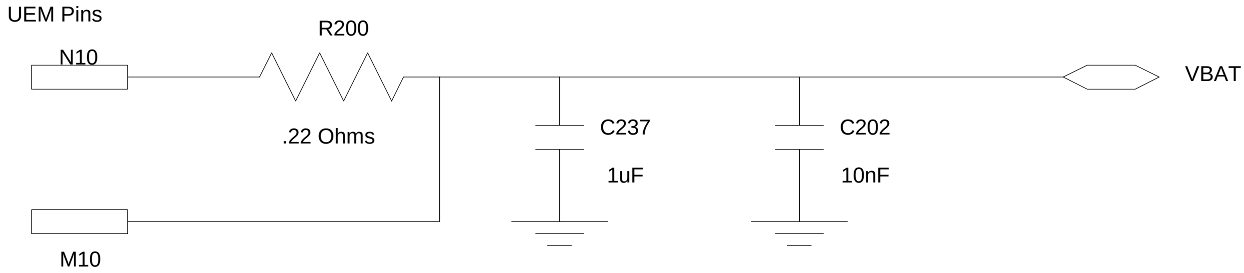


Figure 8: Charging circuit at battery

Audio

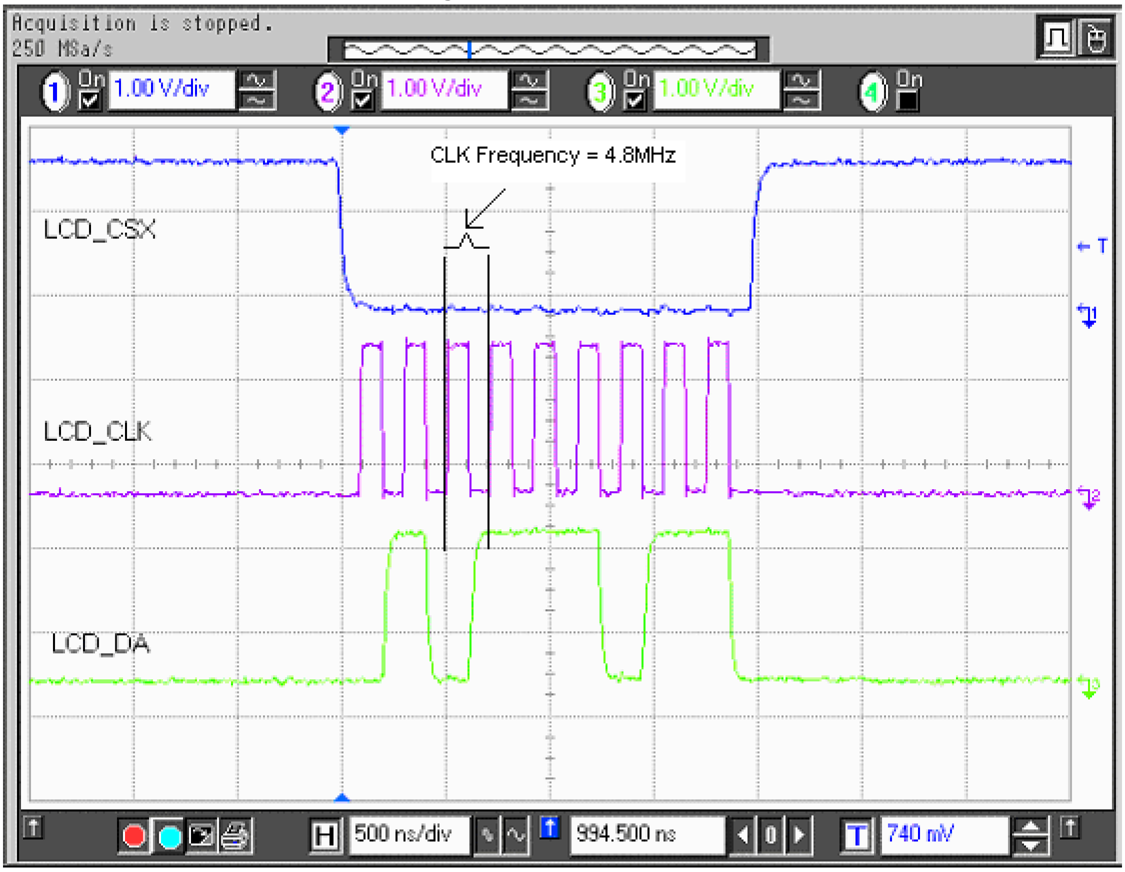
The audio control and processing in RH-34 is supported by UEM, which contains the audio codec, and UPP, which contains the MCU and DSP blocks, handling and processing the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the phone's internal microphone; MIC2 input is used for headsets (HDB-4). MIC3 input is used for the Universal Headset. Every microphone input can have either a differential or single ended AC connection to UEM circuit. In RH-34, the internal microphone MIC1 and external microphone MIC2 for Tomahawk accessory detection are both differential. However, the Universal Headset interface is single-ended. The microphone signals from different sources are connected to separate inputs at UEM. Inputs for the microphone signals are differential type. Also, MICB1 is used for MIC1 and MICB2 is used for MIC2 and MIC3 (Universal Headset).

Display and Keyboard

LEDs are used for LCD and keypad illumination in RH-34. There are three LEDs for the LCD and eight LEDs for the keypad. The signal use to drive the LED driver for the LCD and keyboard is KLIGHT.

Color LCD is used in RH-34. Interface uses 9-bit data transfer. The interface is quite similar to DCT3-type interface, except Command/Data information is transferred together with the data. D/C bit set during each transmitted byte.



FM Radio

FM radio circuitry is implemented using highly integrated radio IC, TEA5767HN. FM radio circuitry is controlled through serial bus (GenIOS) interface by the MCU SW.

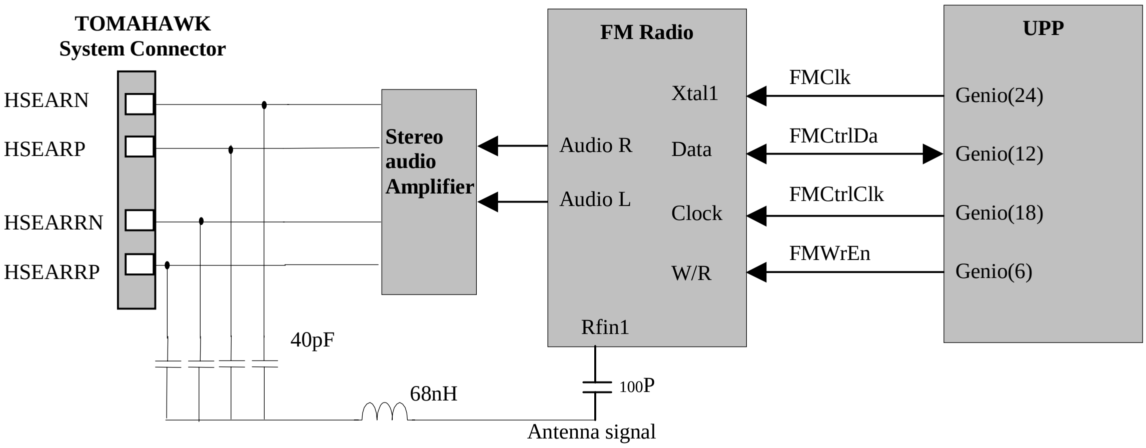


Figure 9: FM Radio (N356) Audio (N150)-, antenna- and digital interface connections

Table 3: FM radio interface timing

FM radio signal	Min	Nom	Max	Condition	Note
FMWrEn	20µs			t_{wd}	FMWrEn high before rising edge of FMCtrlClk (write operation)
FMCtrlClk	 50ms		1 µs	t_r/t_f t_{start}	rise/fall time FMCtrlClk delay after switching on the VFLASH2
FMCtrlDa	 10 µs 1.5 µs 20 µs		14 µs	t_{da} t_{shift} t_{hold} t_{setup}	shift register available after "search ready" data available after FMCtrlClk rising edge (read operation) FMCtrlDa stabile after FMCtrlClk rising edge (write operation) FMCtrlDa set before FMCtrlClk rising edge (write operation)

While WRITE/READ is HIGH the microcontroller can transmit data to the TEA5767. At the rising edge of the Bus clock, the register shifts and accepts the stable bit. At clock low the micro controller writes the following bit. A tuning function is started when the WRITE/READ signal changes from HIGH to LOW. Was a search tuning requested sent, the IC autonomously starts searching the FM band. Search direction and search stop level can be chosen. Was a station with a field strengh equal to or higher than this stop level found, the tuning system stops and the Found Flag bit is set to "HIGH". Was during search a band limit reached, the tuning system stops at the band limit and the Band Limit flag bit is set to high. Also the Found Flag is set to high in this case.

While WRITE/Read is "LOW" data can be read by the UPP. At the rising edge of the BUS Clock, data will be shifted out of the register. This data is available from the point where the bus clock is HIGH until the next rising edge of the clock occurs.

Stereo Audio output signal are fed to Stereo Amplifier. Volume control of the FM audio signal is made by circuitry inside the amplifier. Amplified audio signal is fed to headset or IHF speaker. Headset is also used as antenna input for the radio.

FM Radio Test

To hear the FM radio, you first connect headset to Tomahawk or UHJ ports because the headset will be an FM radio antenna. And you have to connect headset to UHJ port to control the FM radio by using Phoenix. But if you connect a headset (such as HDS-3) to Tomahawk connector, then you can't control the phone because you've already occupied the connection port (Tomahawk), so in this case you have to have jumper wires on production test points (Fbus Tx/RX,GND).

Input signals to FM radio

After connecting a headset to UHJ port to control the phone through Phoenix, you can see below signals by turning on the FM radio in Phoenix. FM radio menu is under RF in Phoenix.

CHECK BELOW FOUR SIGNALS WHETHER THESE ARE CHANGED AS BELOW

FMClk – Test Point (FM04) : 32KHz/1.8V

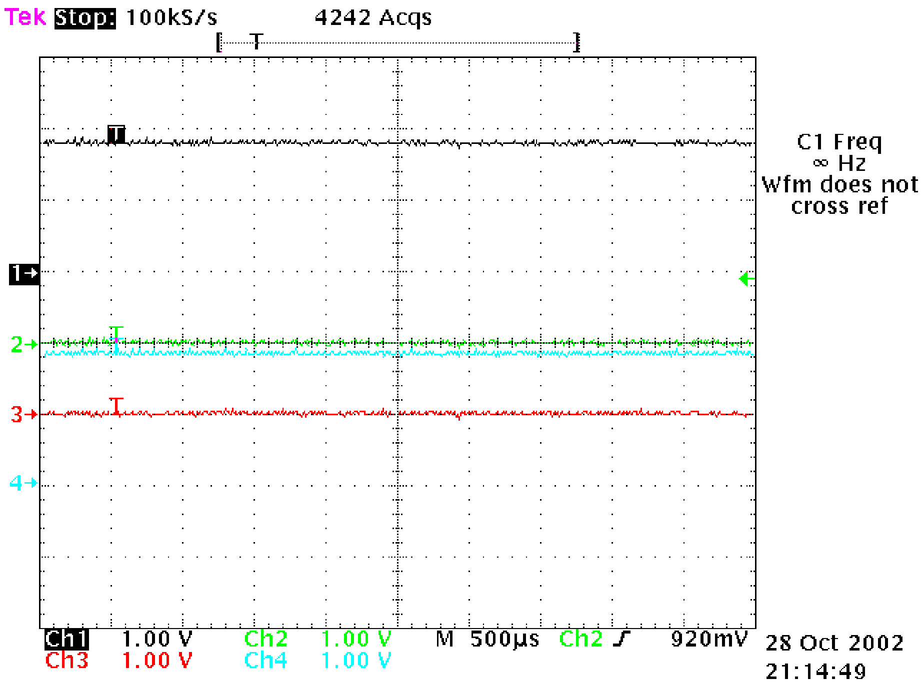
FMWrEn – Test Point (FM03) : Write enable at 1.8V

FMCtrlClk – Test Point (FM02) : Control clock at 1.8V

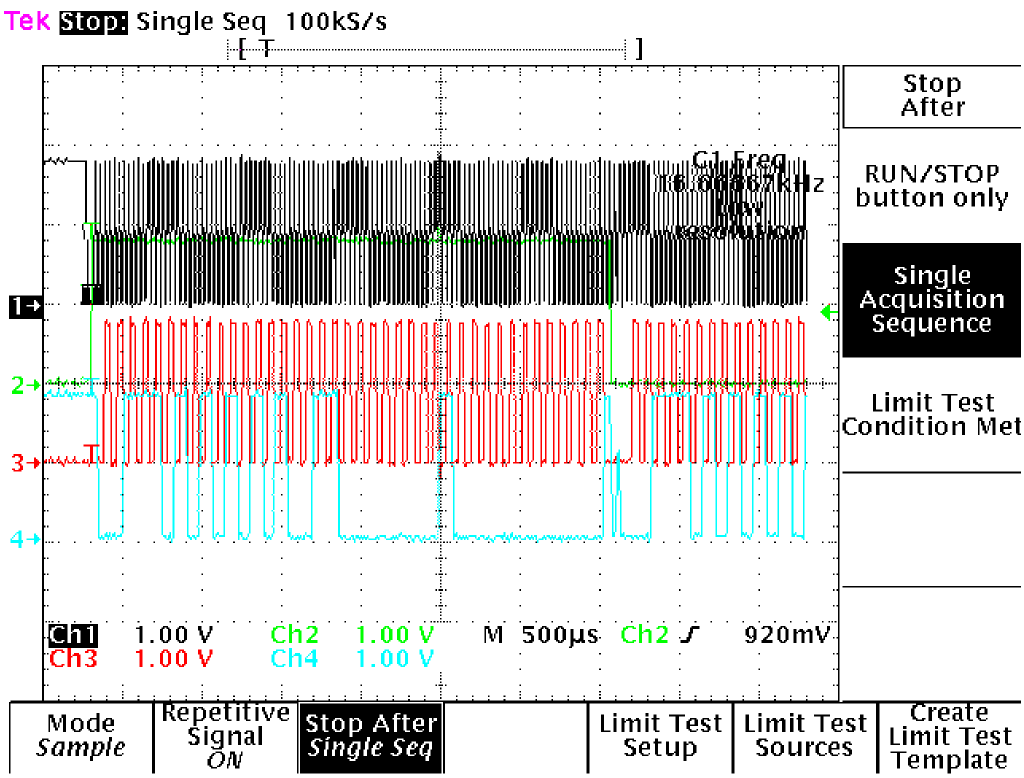
FMCtrlDa – Test Point (FM01) : Control data at 1.8V

FM Radio signals **before** Radio on

Ch1 : FMClk(32.768KHz) , Ch2 : FMWrEn, Ch3 : FMctrlClk, Ch4 : FMctrlDA



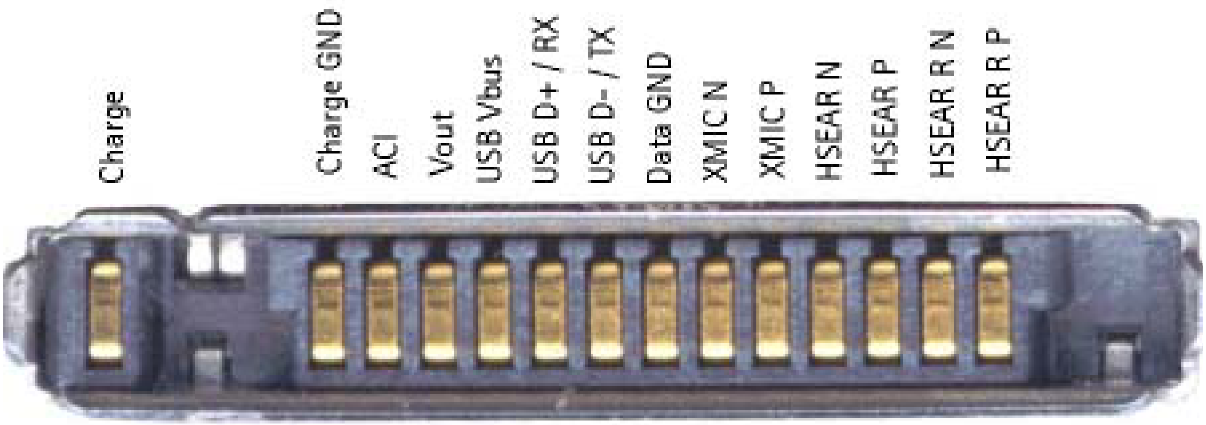
FM Radio signals **after** Radio on



Accessory

RH-34 is designed to support Tomahawk and Universal Headset accessories, differential and single-ended, respectively. Detection of Tomahawk accessories is done through the ACI signal where the Universal Headset is detected on GenIO (21).

The following picture shows the pin out of the Tomahawk connector.



The pin out on the Tomahawk connector is as follows:

1 Charger

2 Charger GND

3 ACI

4 Vout

5 USB Vbus

6 USB D+ / Fbus Rx

7 USB D- / Fbus Tx

8 Data GND

9 XMic N

10 XMic P

11 HSear N

12 HSear P

13 HSear R N

14 HSear R P

In Tomahawk accessories, perform the following functions: Charging, Accessory detection, FBUS communication, USB communication, and fully differential audio interface for mono and stereo outputs. These modes are explained in the following sections.

Charging

Charging through the Tomahawk is done same way as through the charger connector. Pin 1 of the Tomahawk is physically connected the charger connector. So when the phone is connected to the desktop charger such as the DCV-15, it is charged the same way as is done on the charger connector.

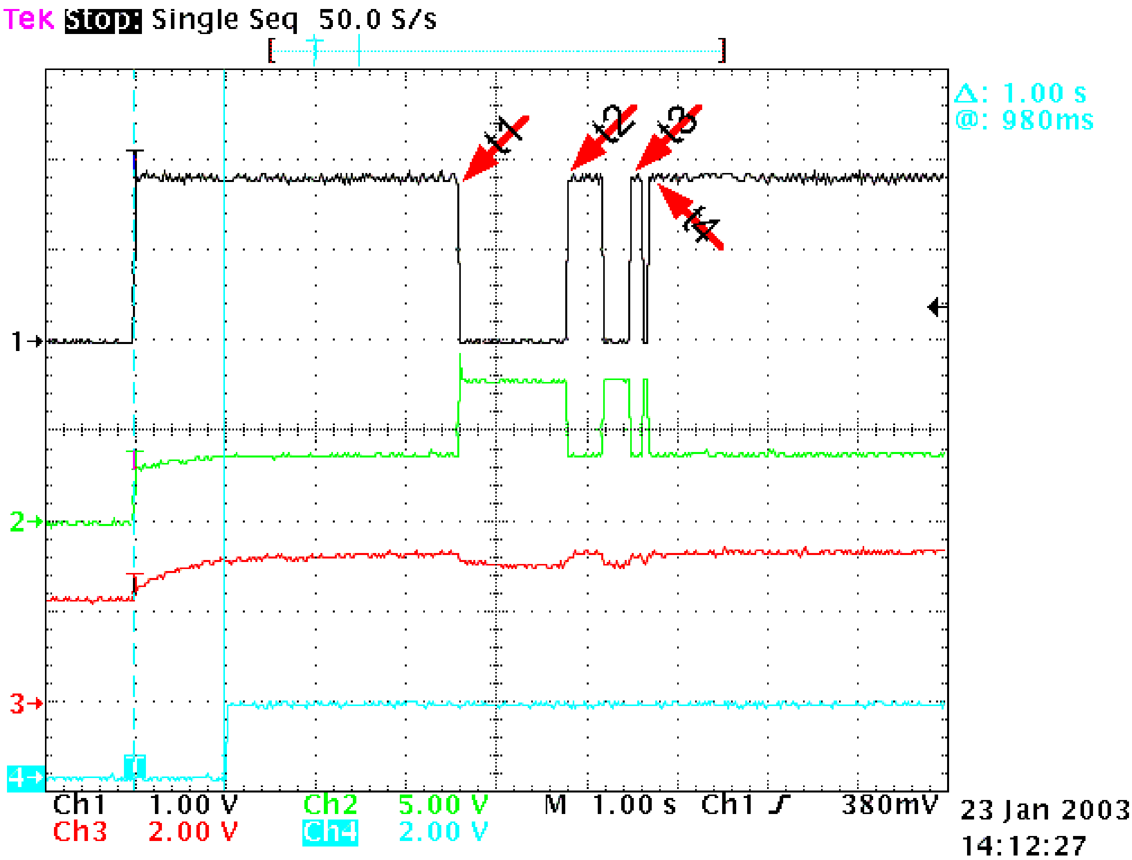
The actual charging sequence can be seen in the following figure. The channels on the figure are as follows:

CH1 = Charging current across the .22 Ohm (R200) resistor on UEMK

CH2 = Charger voltage measure at V100

CH3 = Battery voltage measure at R200

CH4 = PURX



t1: UEM opens charge switch and UPP startup.
t2: This is very very early in phone SW startup where the charge switch is being closed.
Charge switch remains closed during OS and server startup to prevent HW cut-off.
t3: EM SW is started and charger recognition SW verifies charger current.
t4: Charger is accepted and Constant Current charging is started.

In Channel 4, we can see that PURX is release and this is when the phone operation goes from "RESET" mode to "POWER_ON" mode.

Tomahawk headset detection

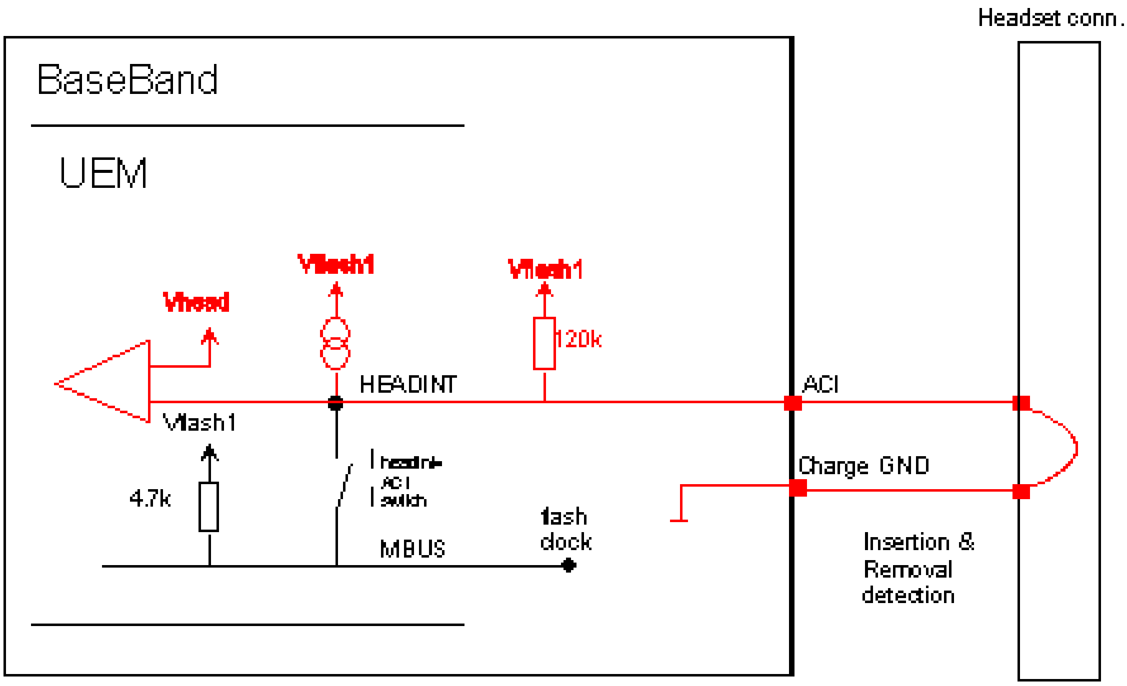
Accessory detection on Tomahawk is done digitally. The pins used for accessory detection are:

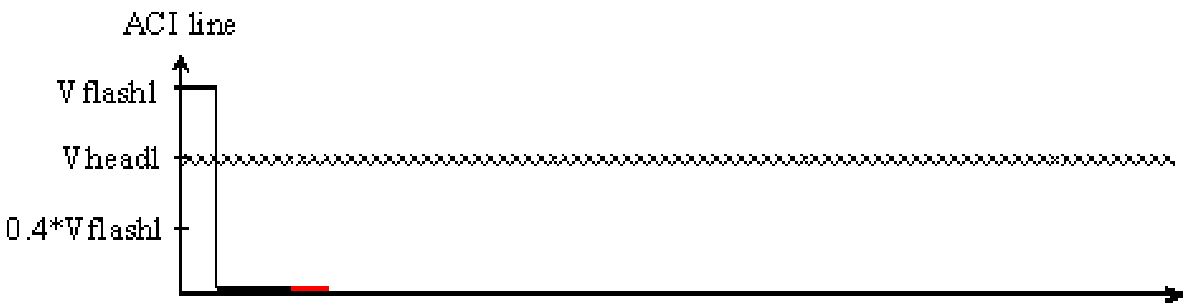
Pin 2 (Charge GND)

Pin 3 (ACI)

Pin 4 (Vout)

A waveform of such detection can be seen in the following figure:





FBus detection

FBus communication in Tomahawk is done through the following lines:

Pin 2 (Charge GND)

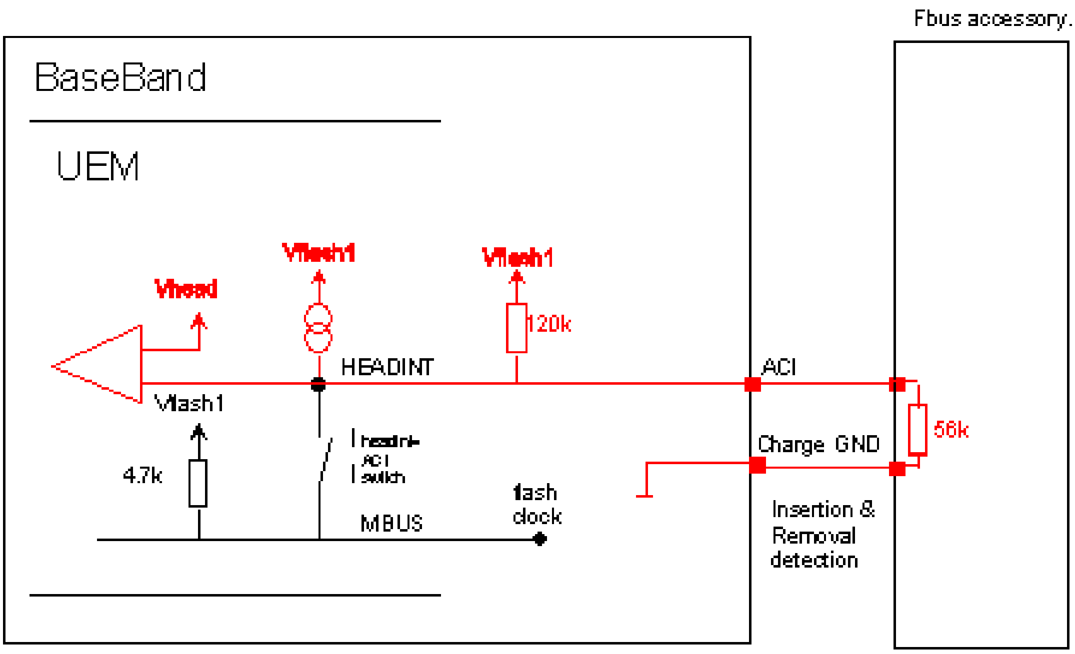
Pin 3 (ACI)

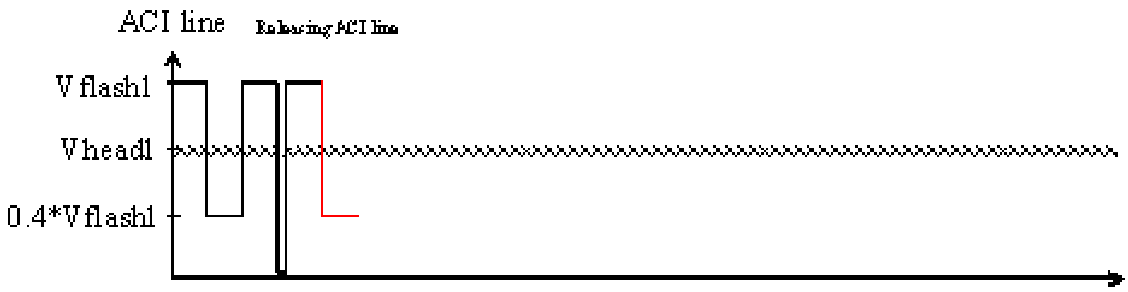
Pin 4 (Vout)

Pin 6 (FBus Rx)

Pin 7 (FBus Tx)

A waveform for such communication is shown in the following figure:



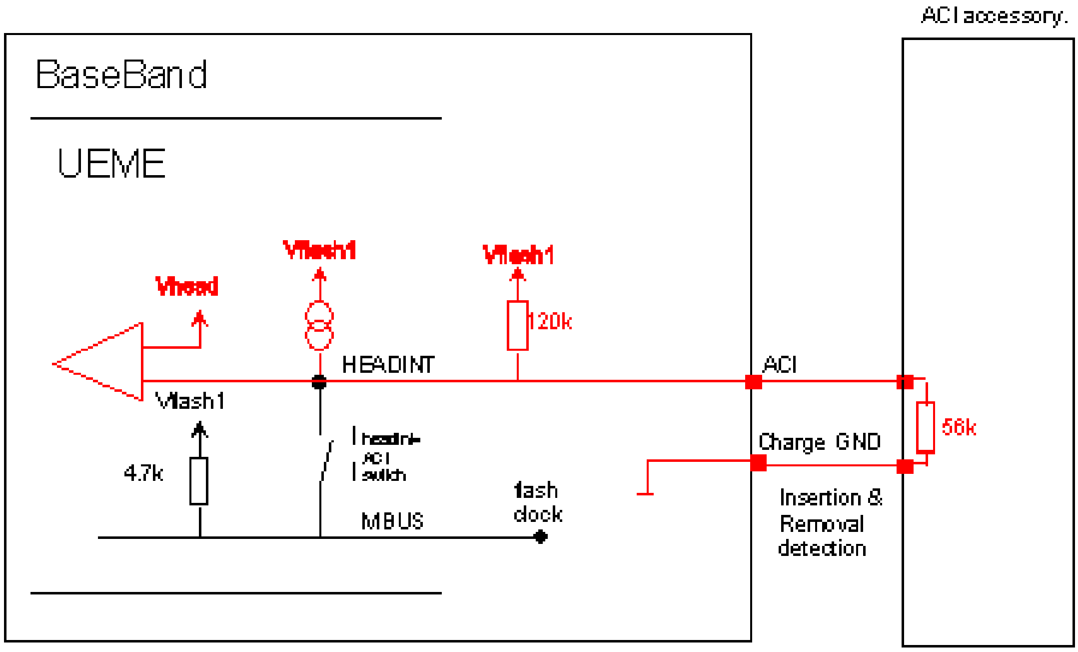


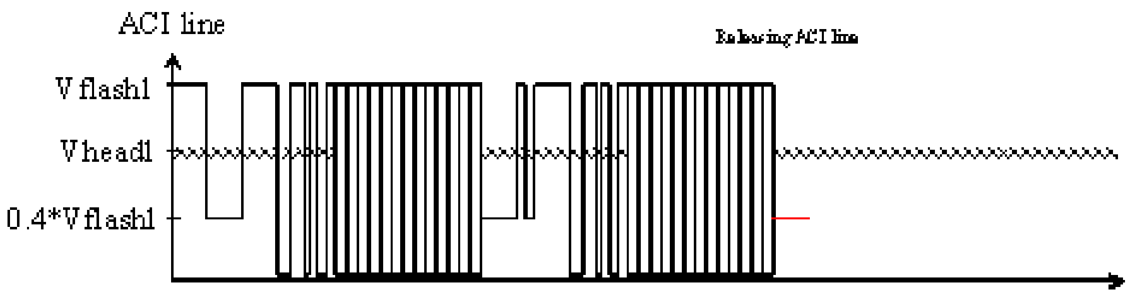
Accessory detection though ACI

USB and Audi on (mono or stereo) and FM radio communication in Tomahawk is done through the following signals:

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

A waveform showing such interface is shown in the following figure:





RUIM (SIM CAR)

RH-34 supports RUIM for China products. The following waveform can be used to verify that sim_vcc; sim_i/o, sim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture can be taken when the RUIM is installed on the phone and measures the signals when the phone is turned on. The following picture shows the proper waveforms when the interface is working. See “Bottom view” diagram for the test point locations.

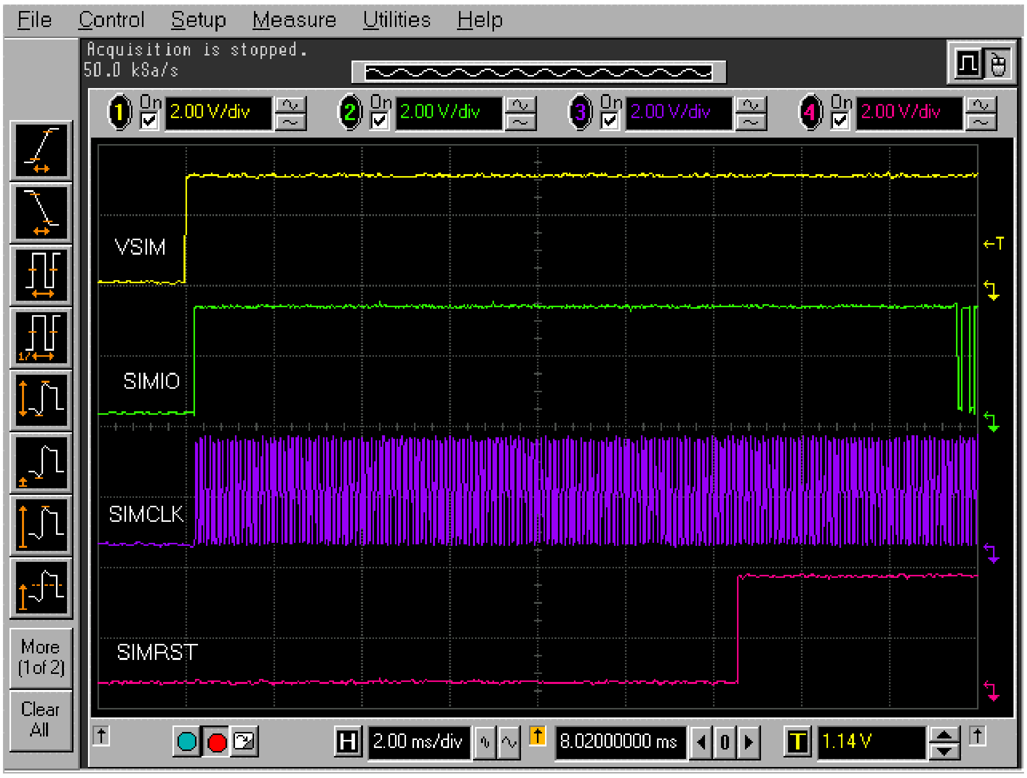
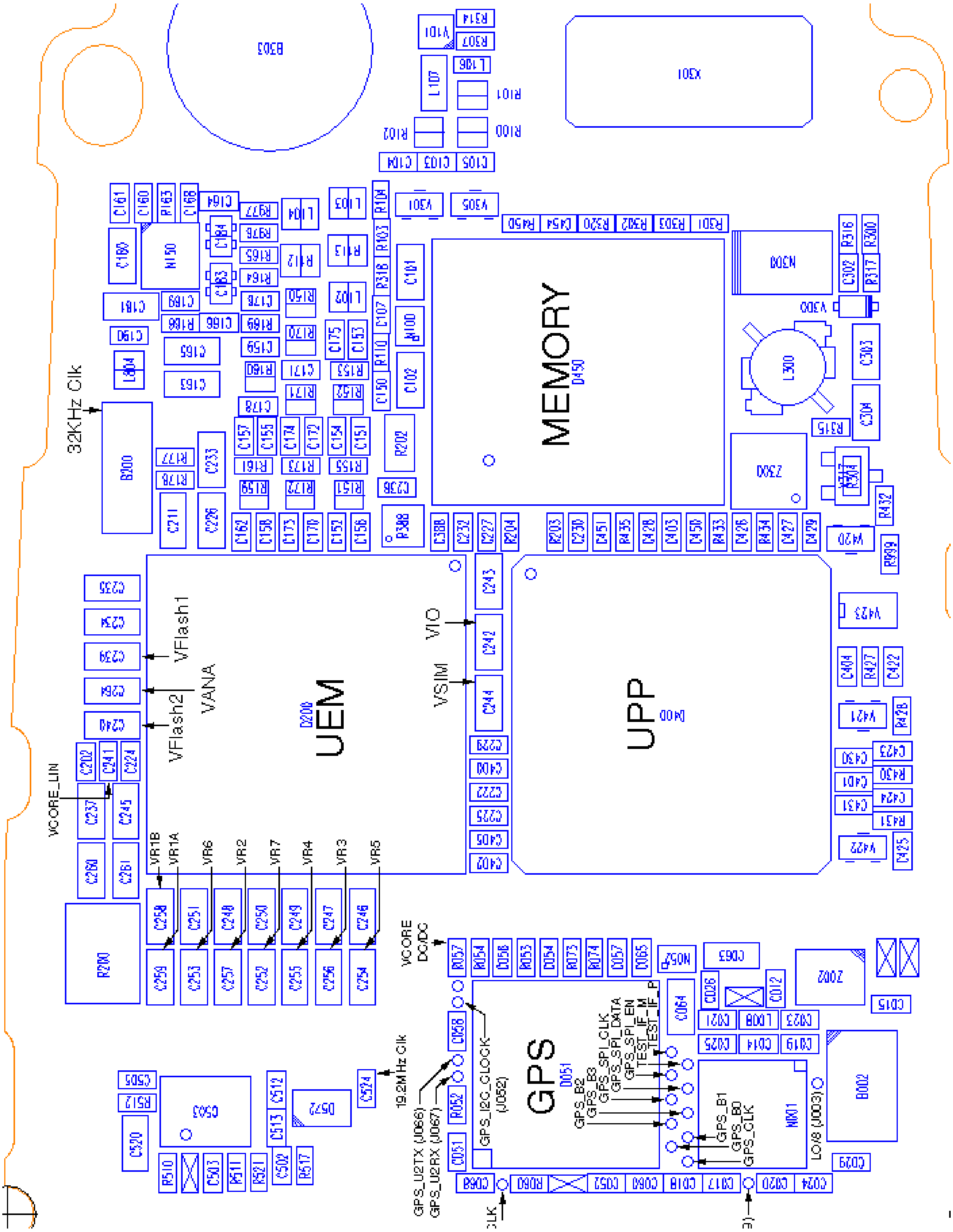


Figure 10: RUIM signal waveform

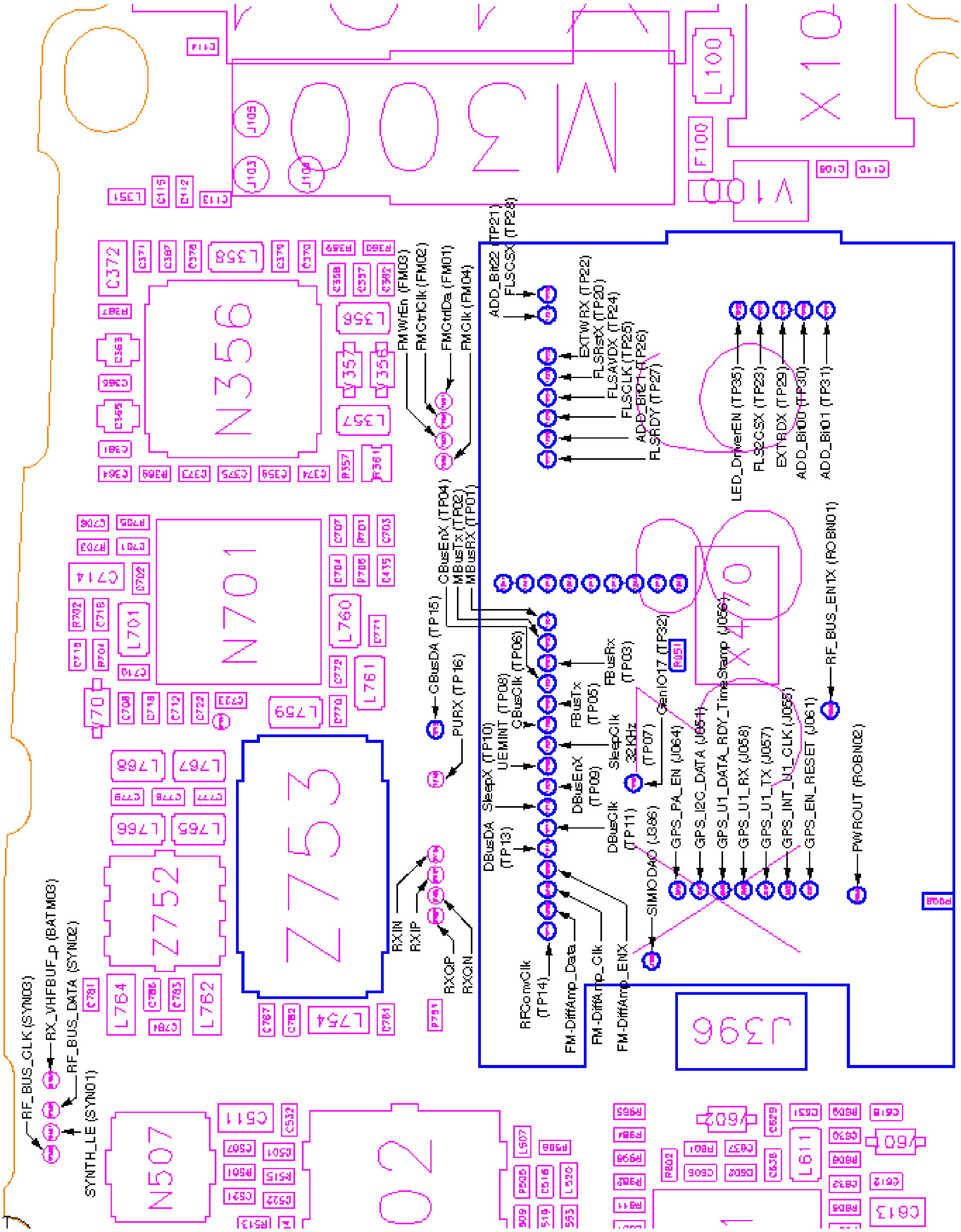
Test Points

RH-34 BB test points, regulators, and BB ASICs.

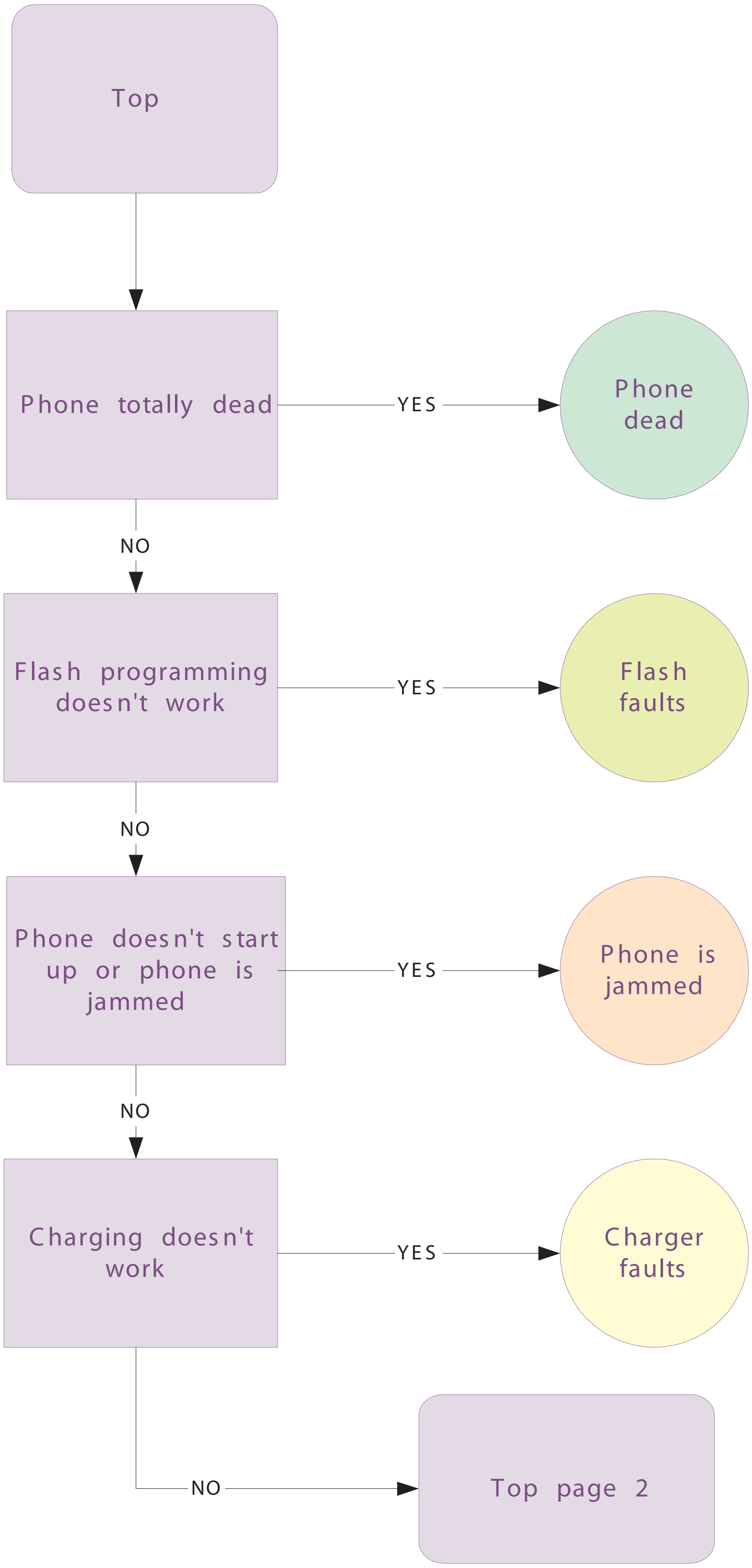
Top view

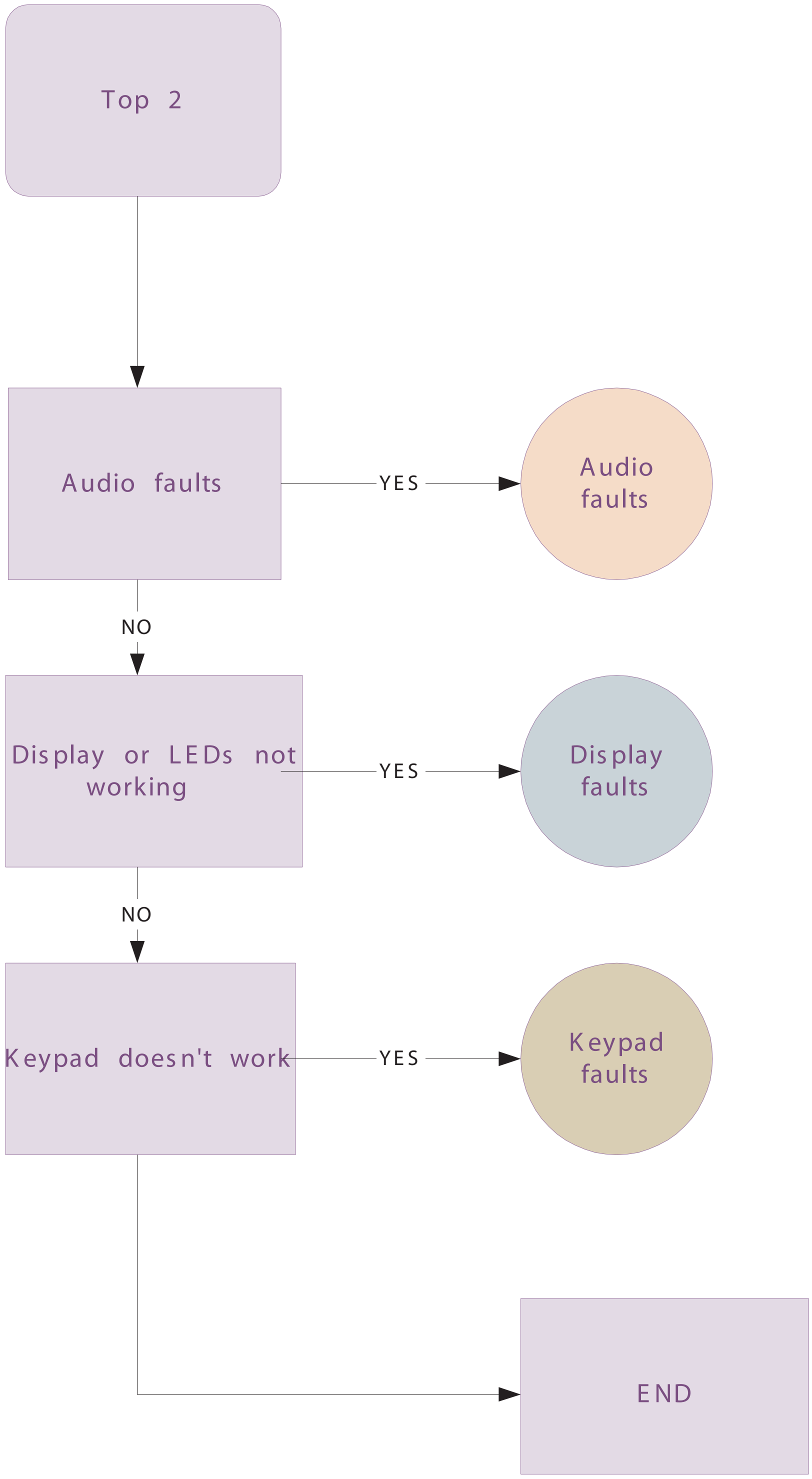

MEMORY
D450
UEM
D200
UPP
GPS
D051
32KHz Clk
VFlash1
VANA
VFlash2
VIO
VSIM
VCORE_LIN
VCORE DC/DC
19.2MHz Clk
GPS_U2TX (J066)
GPS_U2RX (J067)
GPS_I2C_CLOCK (J052)
GPS_B2
GPS_B3
GPS_SPI_CLK
GPS_SPI_DATA
GPS_SPI_EN
TEST_IF_M
TEST_IF_P
GPS_B1
GPS_B0
GPS_CLK
LO/8 (J003)
VR1B
VR1A
VR6
VR2
VR7
VR4
VR3
VR5

Bottom view

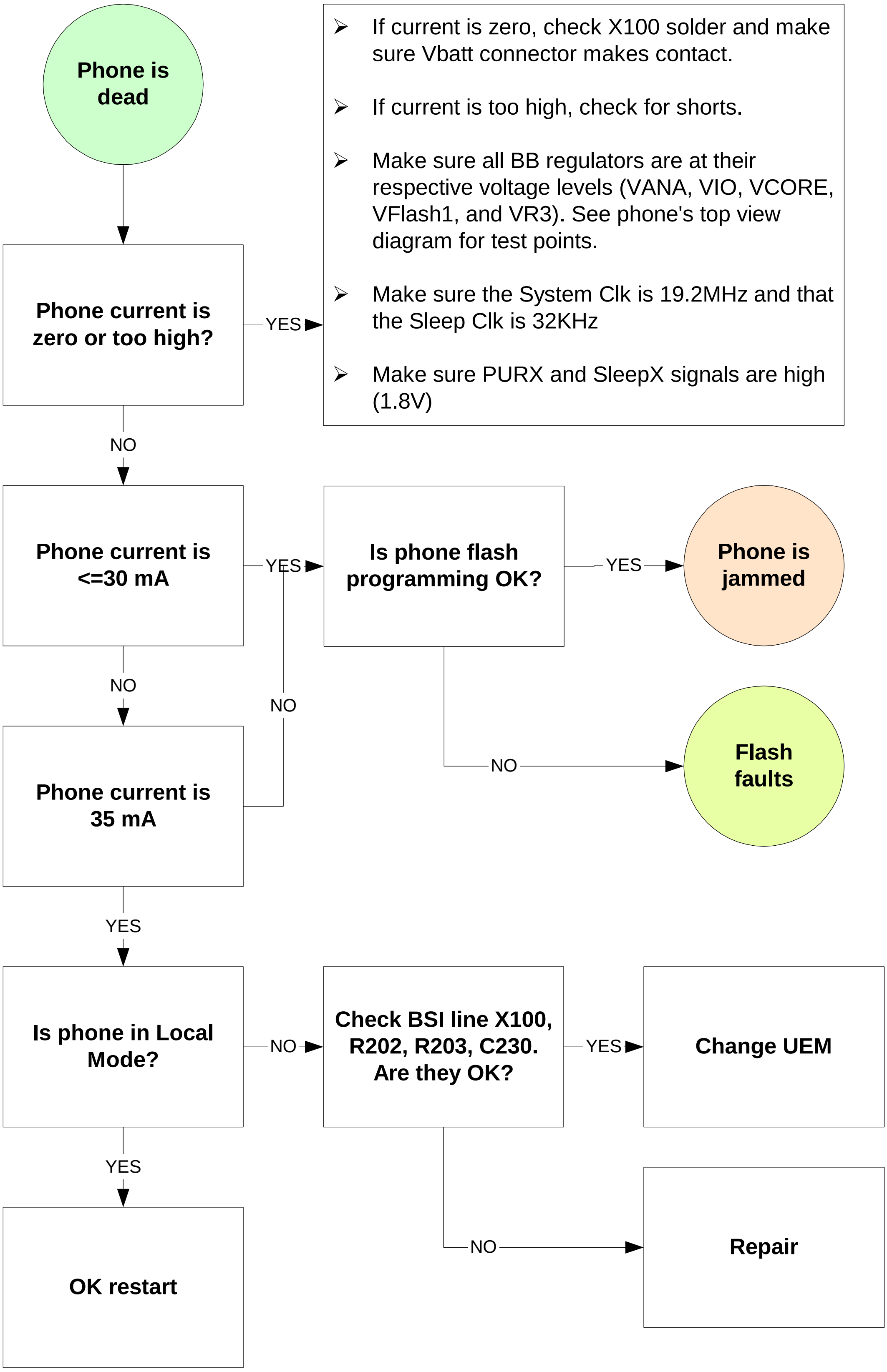

RF_BUS_CLK (SYNC03)
RX_VHFBUF_p (BATM03)
RF_BUS_DATA (SYNC02)
SYNTH_LE (SYNC01)
RXIN
RXIP
RXQP
RXQN
PURX (TP16)
CBusDA (TP15)
CBusEnX (TP04)
MBusTx (TP02)
MBusRx (TP01)
FMWrEn (FM03)
FMCtrlClk (FM02)
FMCtrlDa (FM01)
FMClk (FM04)
ADD_Bit22 (TP21)
FLSCSX (TP28)
EXTWRX (TP22)
FLSRstX (TP20)
FLSAVDX (TP24)
FLSCLK (TP25)
ADD_Bit21 (TP26)
FLSRDY (TP27)
LED_DriverEN (TP35)
FLS2CSX (TP23)
EXTRDX (TP29)
ADD_Bit00 (TP30)
ADD_Bit01 (TP31)
RF_BUS_EN1X (ROBN01)
PWROUT (ROBN02)
DBusDA (TP13)
SleepX (TP10)
UEMINT (TP08)
CBusClk (TP06)
FBusTx (TP05)
FBusRx (TP03)
DBusEnX (TP09)
SleepClk 32kHz (TP07)
GenIO17 (TP32)
DBusClk (TP11)
SIMIODAO (J386)
GPS_PA_EN (J064)
GPS_I2C_DATA (J051)
GPS_U1_RX (J058)
GPS_U1_TX (J057)
GPS_INT_U1_CLK (J055)
GPS_EN_RESET (J061)
RFConvClk (TP14)
FM-DiffAmp_Data
FM-DiffAmp_Clk
FM-DiffAmp_ENX

Top troubleshooting map

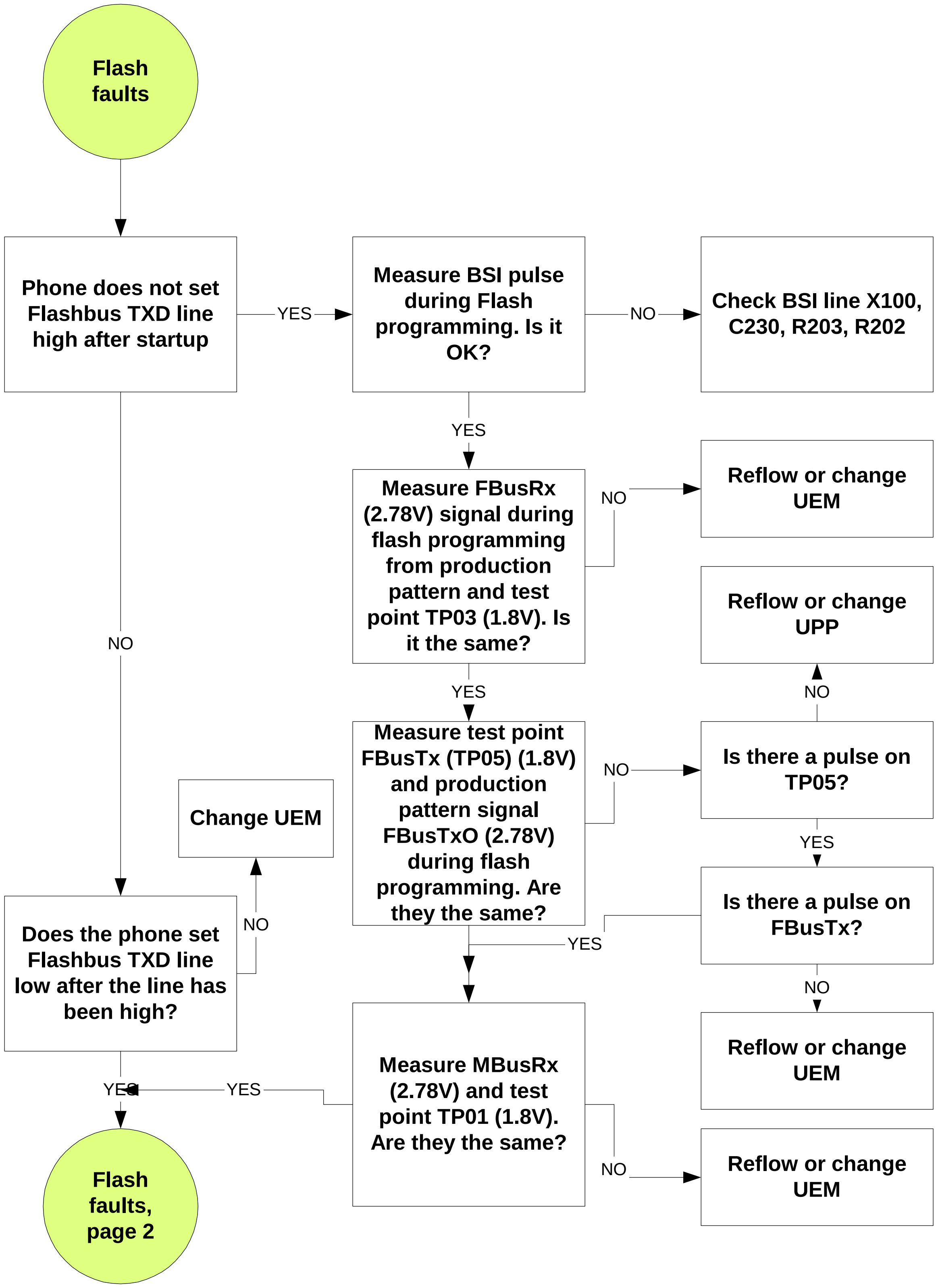


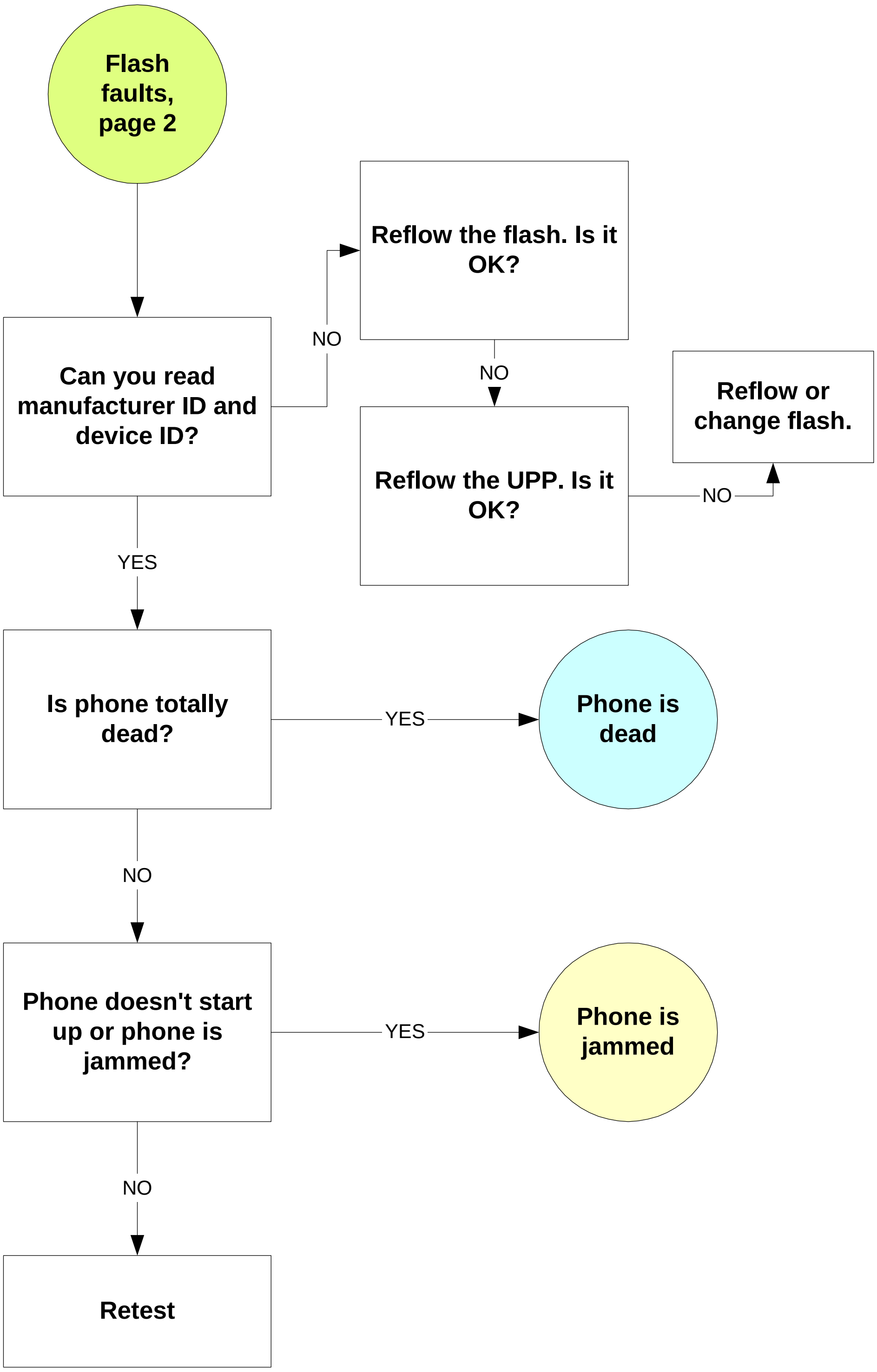

Top 2
Audio faults
YES
Audio faults
NO
Display or LEDs not working
YES
Display faults
NO
Keypad doesn't work
YES
Keypad faults
END

Phone is totally dead

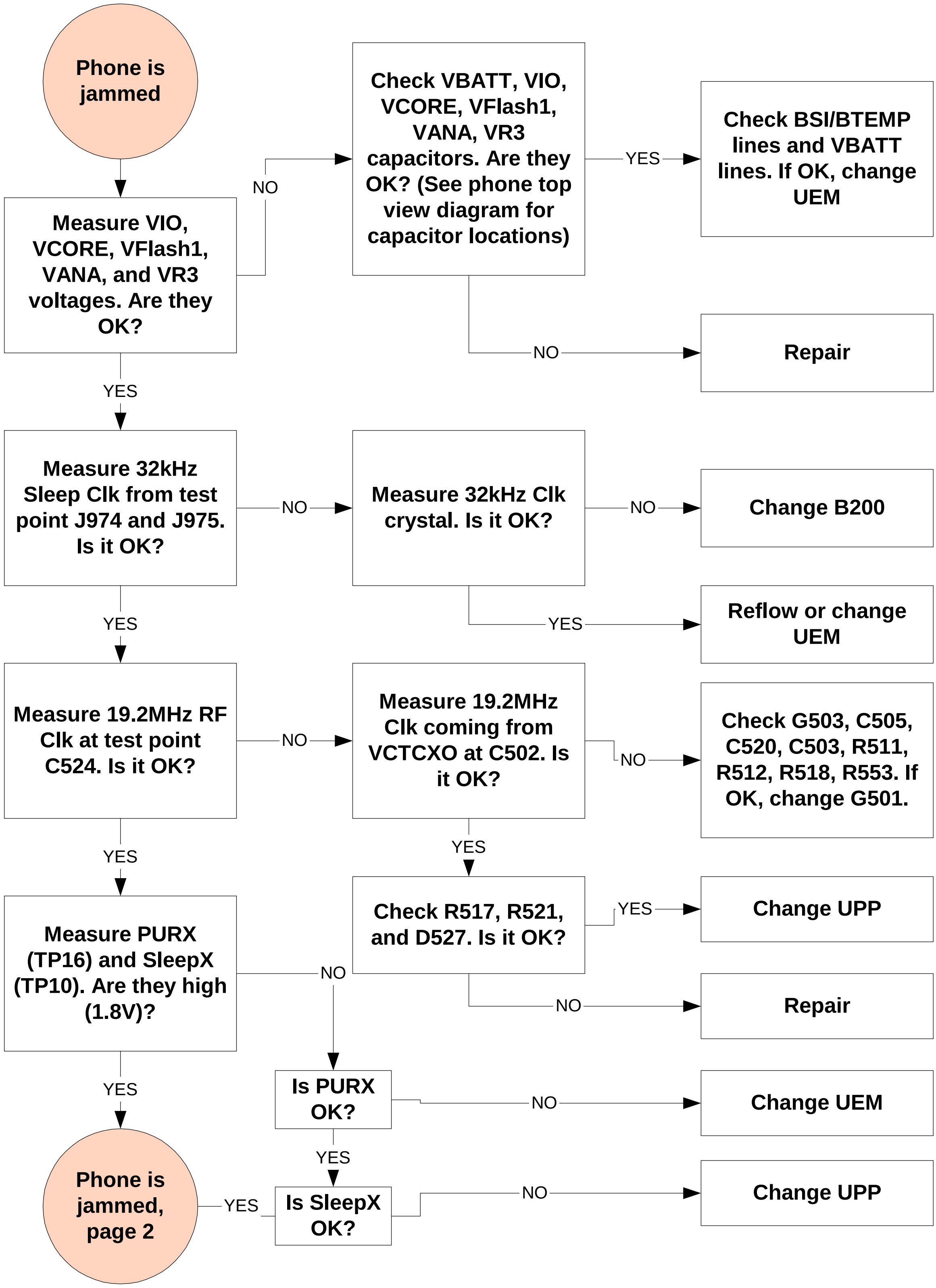


Flash programming doesn't work

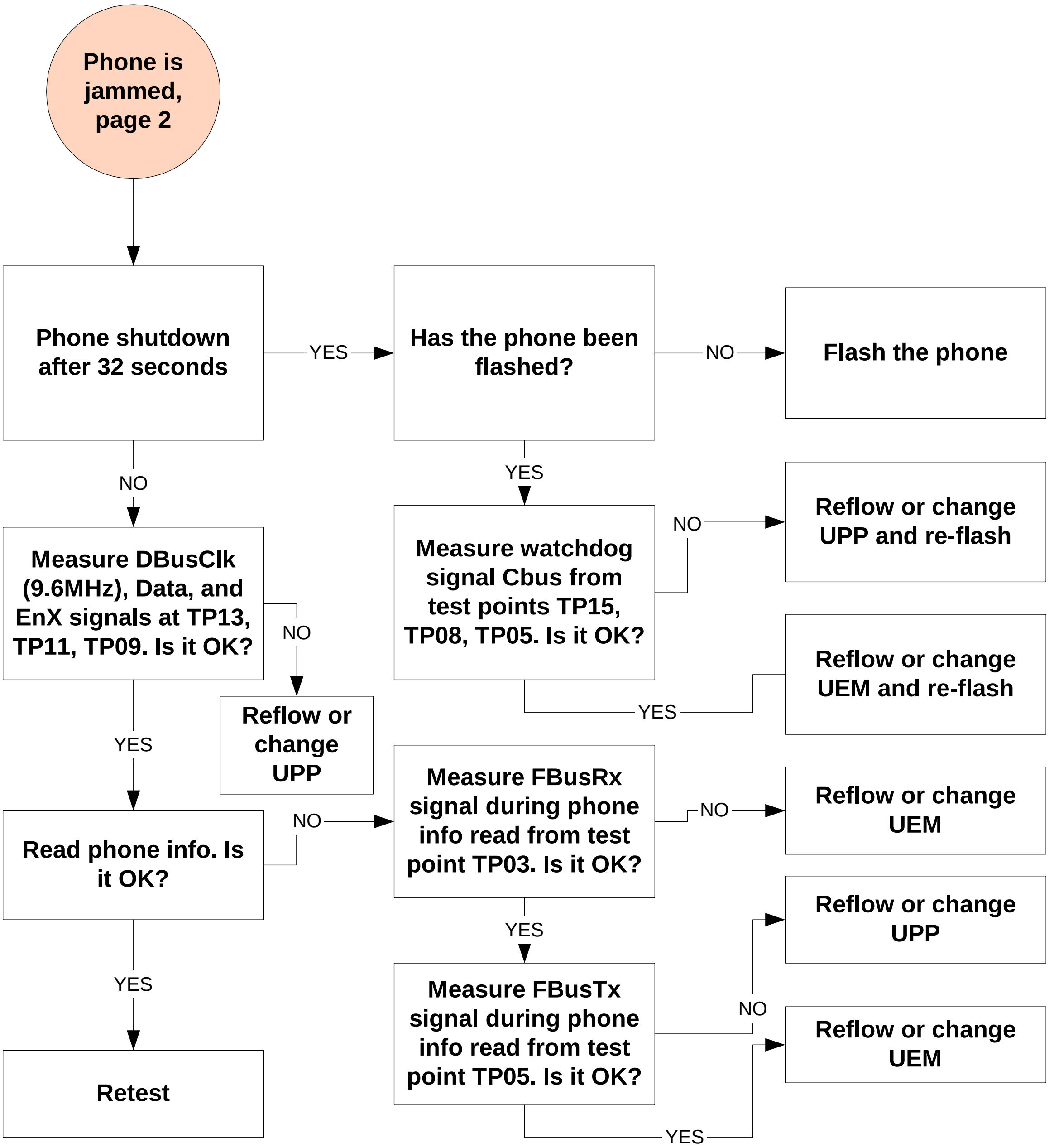



Flash faults, page 2
Can you read manufacturer ID and device ID?
NO
Reflow the flash. Is it OK?
NO
Reflow the UPP. Is it OK?
NO
Reflow or change flash.
YES
Is phone totally dead?
YES
Phone is dead
NO
Phone doesn't start up or phone is jammed?
YES
Phone is jammed
NO
Retest

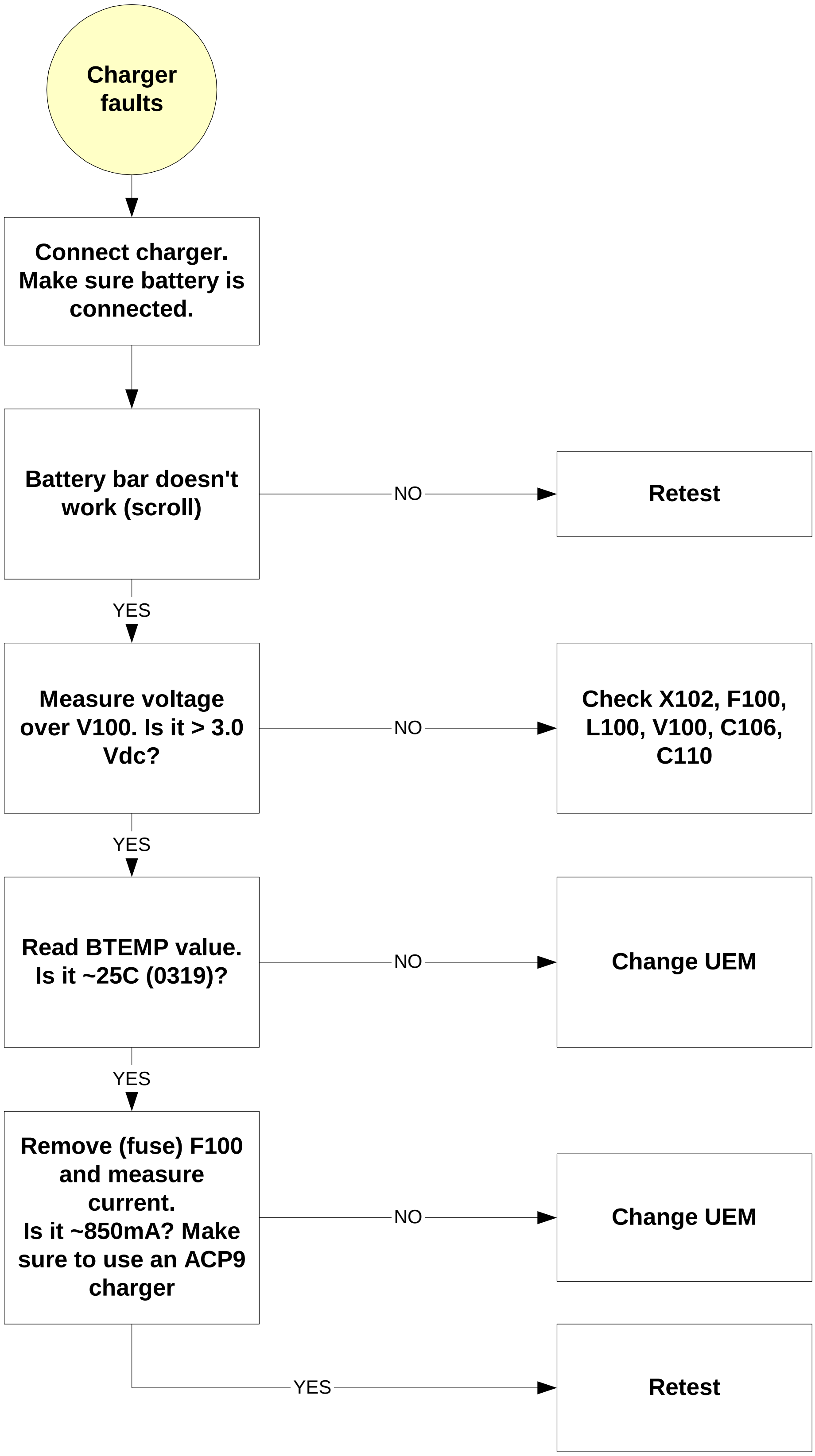
Phone is jammed



Power doesn't stay on or the phone is jammed

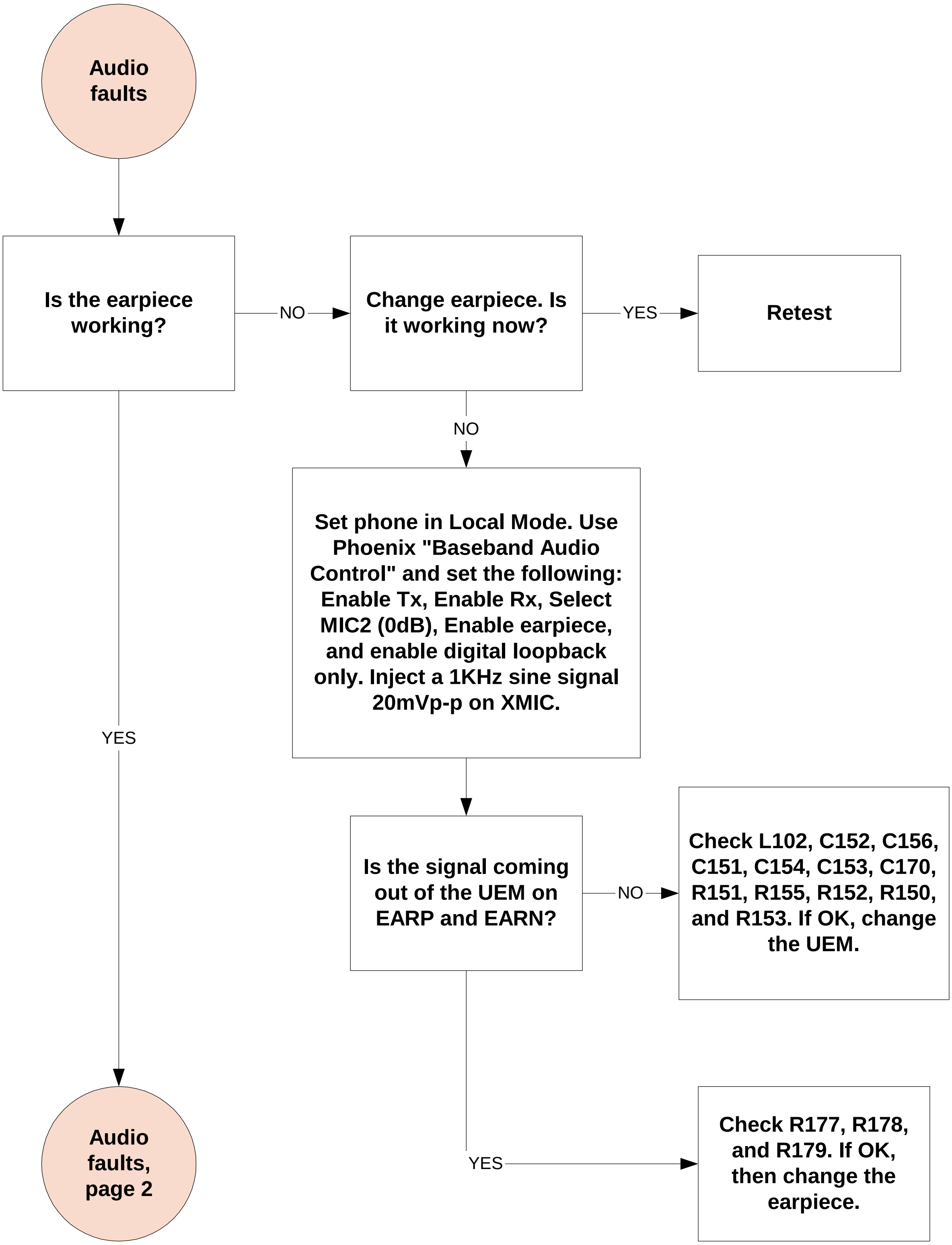


Charger faults

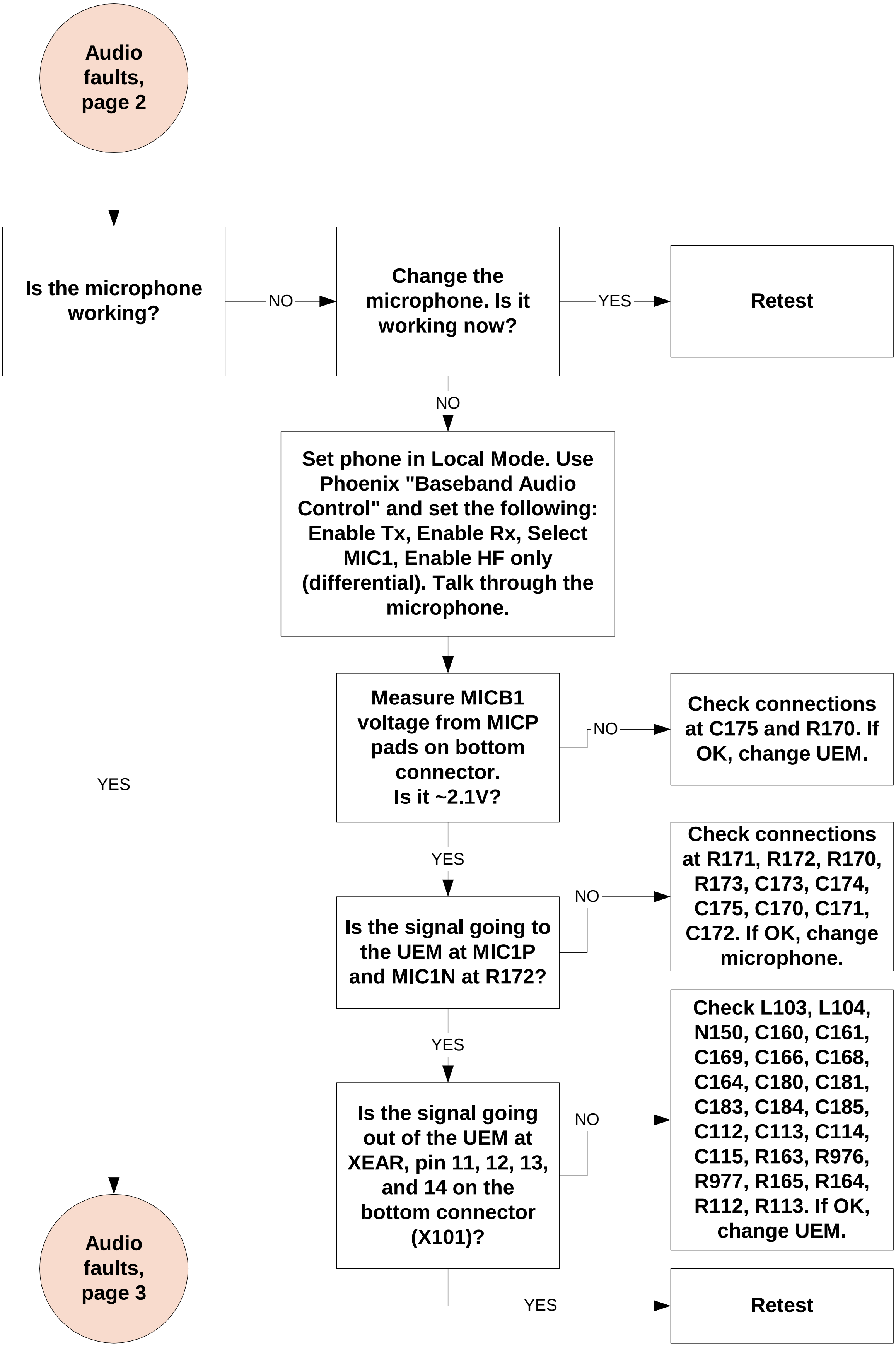


Audio faults

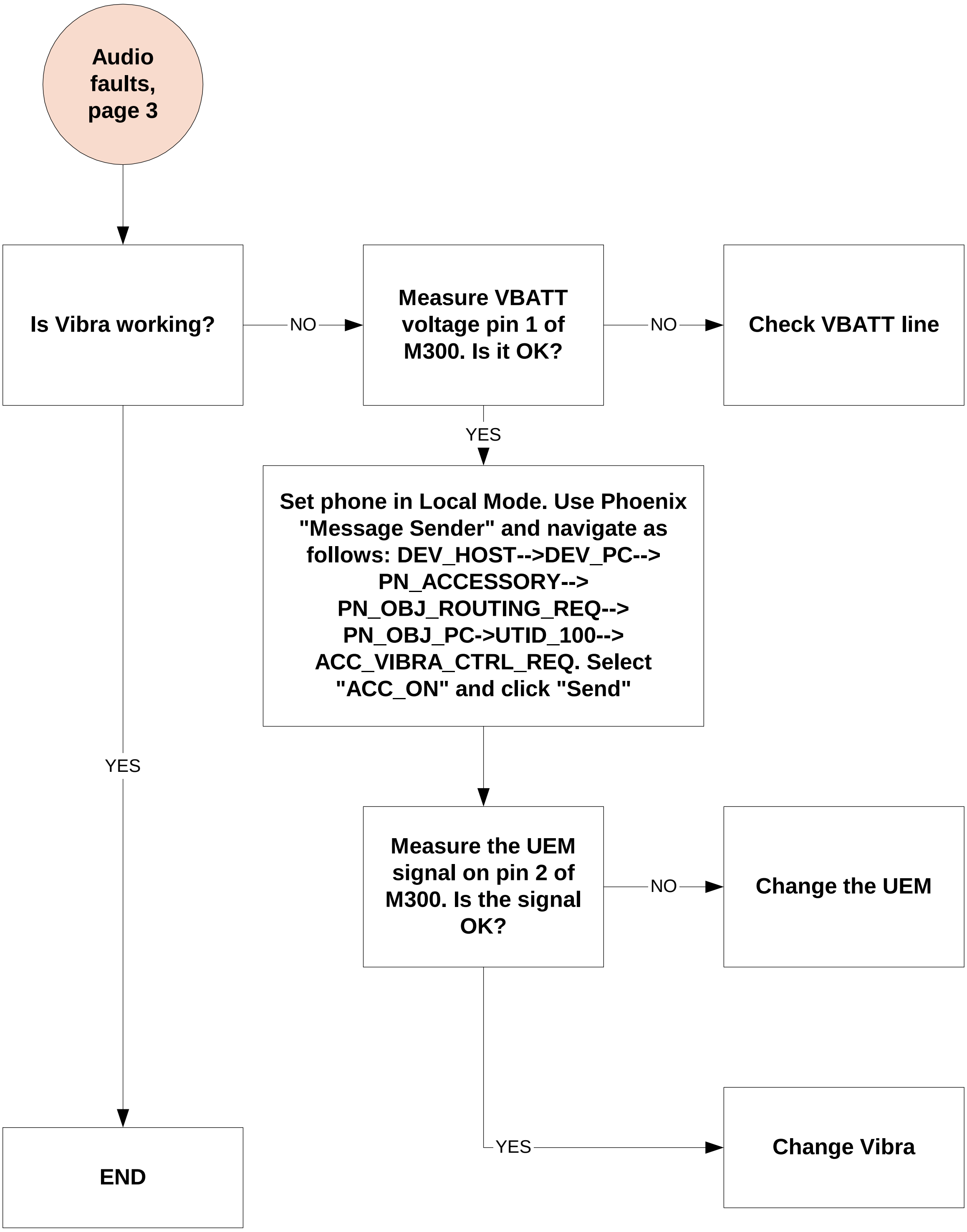
Earpiece



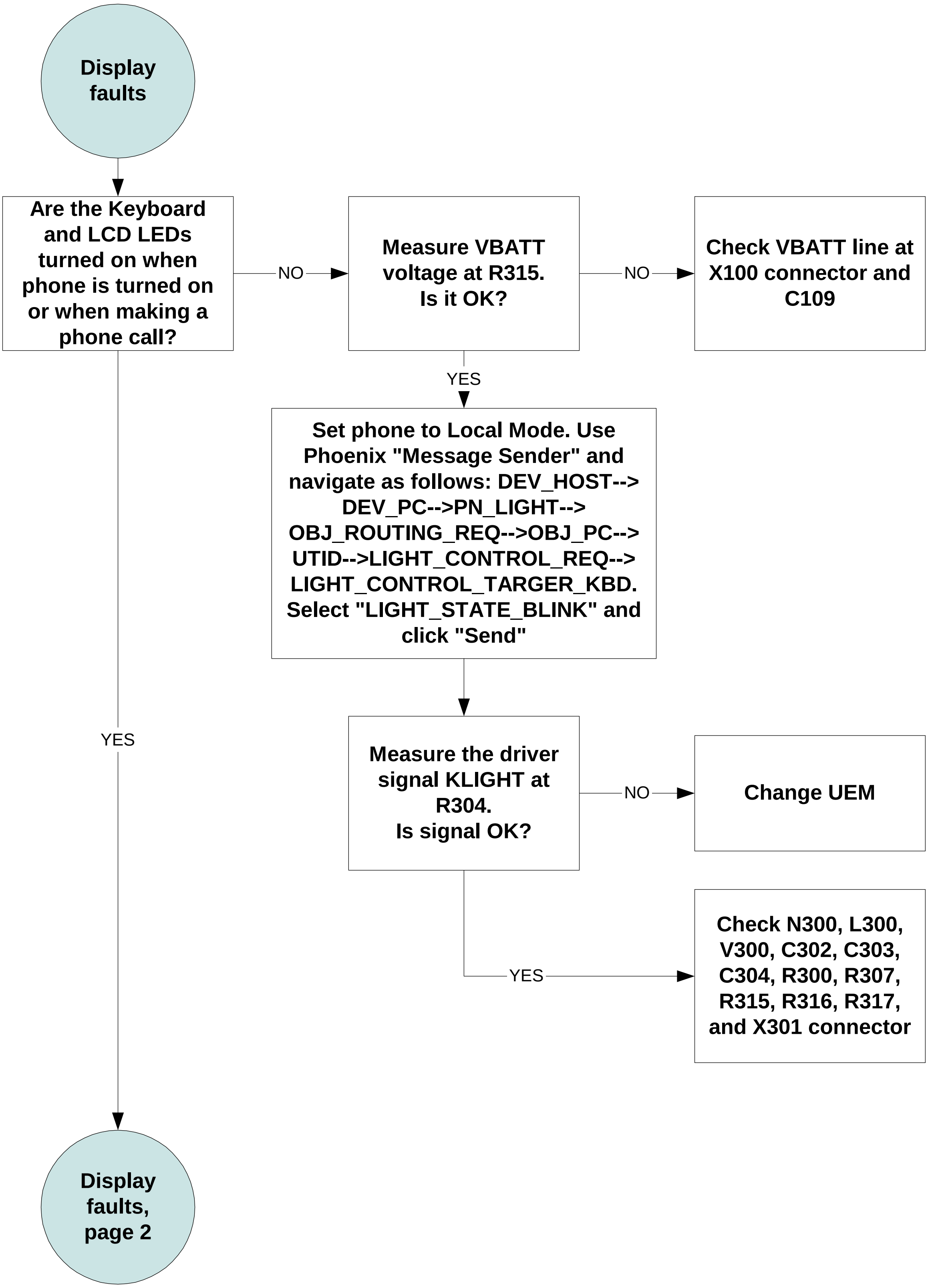
Microphone

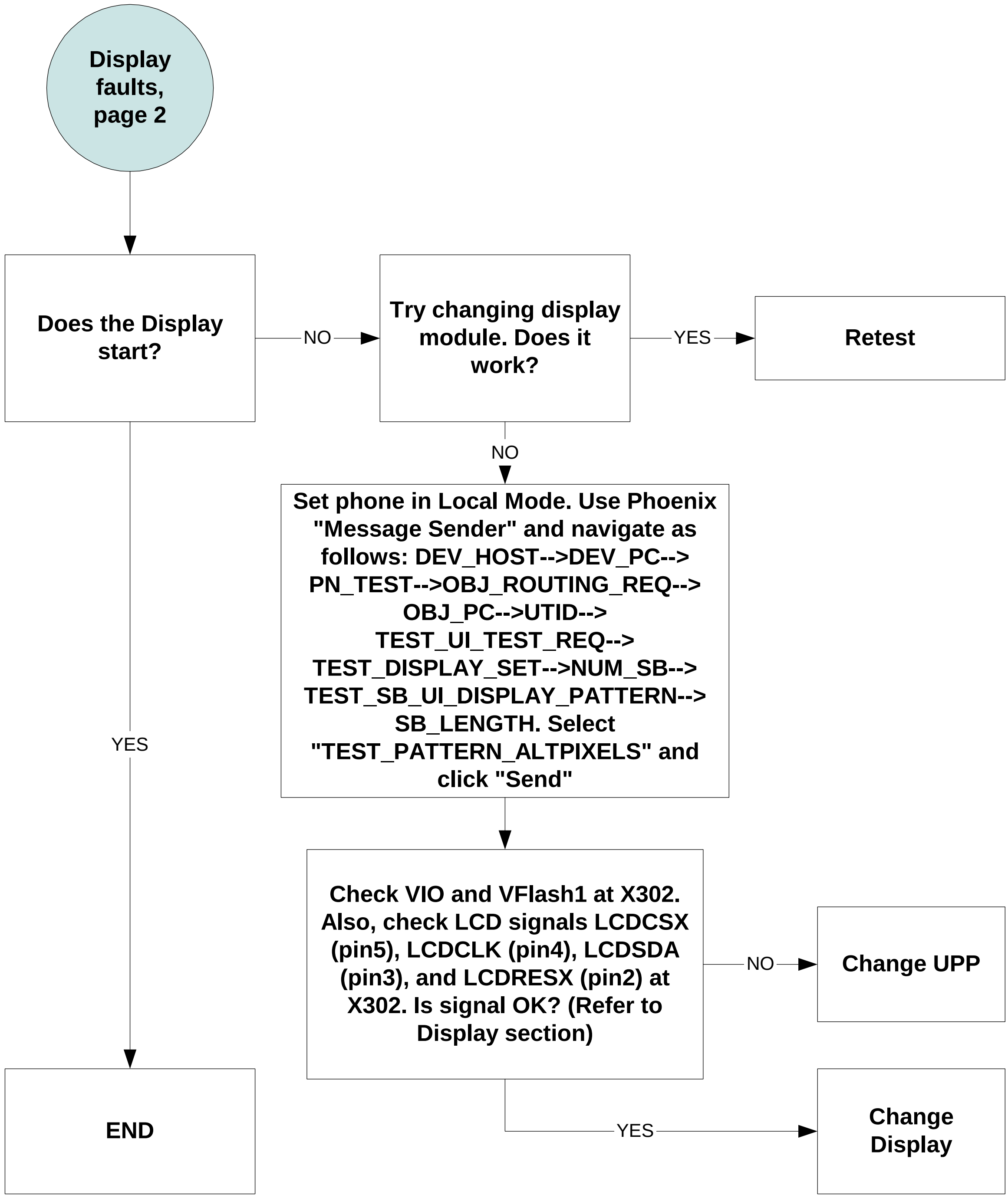

Audio faults, page 2
Is the microphone working?
NO
Change the microphone. Is it working now?
YES
Retest
NO
Set phone in Local Mode. Use Phoenix "Baseband Audio Control" and set the following: Enable Tx, Enable Rx, Select MIC1, Enable HF only (differential). Talk through the microphone.
Measure MICB1 voltage from MICP pads on bottom connector. Is it ~2.1V?
NO
Check connections at C175 and R170. If OK, change UEM.
YES
Is the signal going to the UEM at MIC1P and MIC1N at R172?
NO
Check connections at R171, R172, R170, R173, C173, C174, C175, C170, C171, C172. If OK, change microphone.
YES
Is the signal going out of the UEM at XEAR, pin 11, 12, 13, and 14 on the bottom connector (X101)?
NO
Check L103, L104, N150, C160, C161, C169, C166, C168, C164, C180, C181, C183, C184, C185, C112, C113, C114, C115, R163, R976, R977, R165, R164, R112, R113. If OK, change UEM.
YES
Retest
YES
Audio faults, page 3

Vibra


Audio faults, page 3
Is Vibra working?
NO
Measure VBATT voltage pin 1 of M300. Is it OK?
NO
Check VBATT line
YES
Set phone in Local Mode. Use Phoenix "Message Sender" and navigate as follows: DEV_HOST-->DEV_PC--> PN_ACCESSORY--> PN_OBJ_ROUTING_REQ--> PN_OBJ_PC->UTID_100--> ACC_VIBRA_CTRL_REQ. Select "ACC_ON" and click "Send"
YES
Measure the UEM signal on pin 2 of M300. Is the signal OK?
NO
Change the UEM
YES
Change Vibra
END

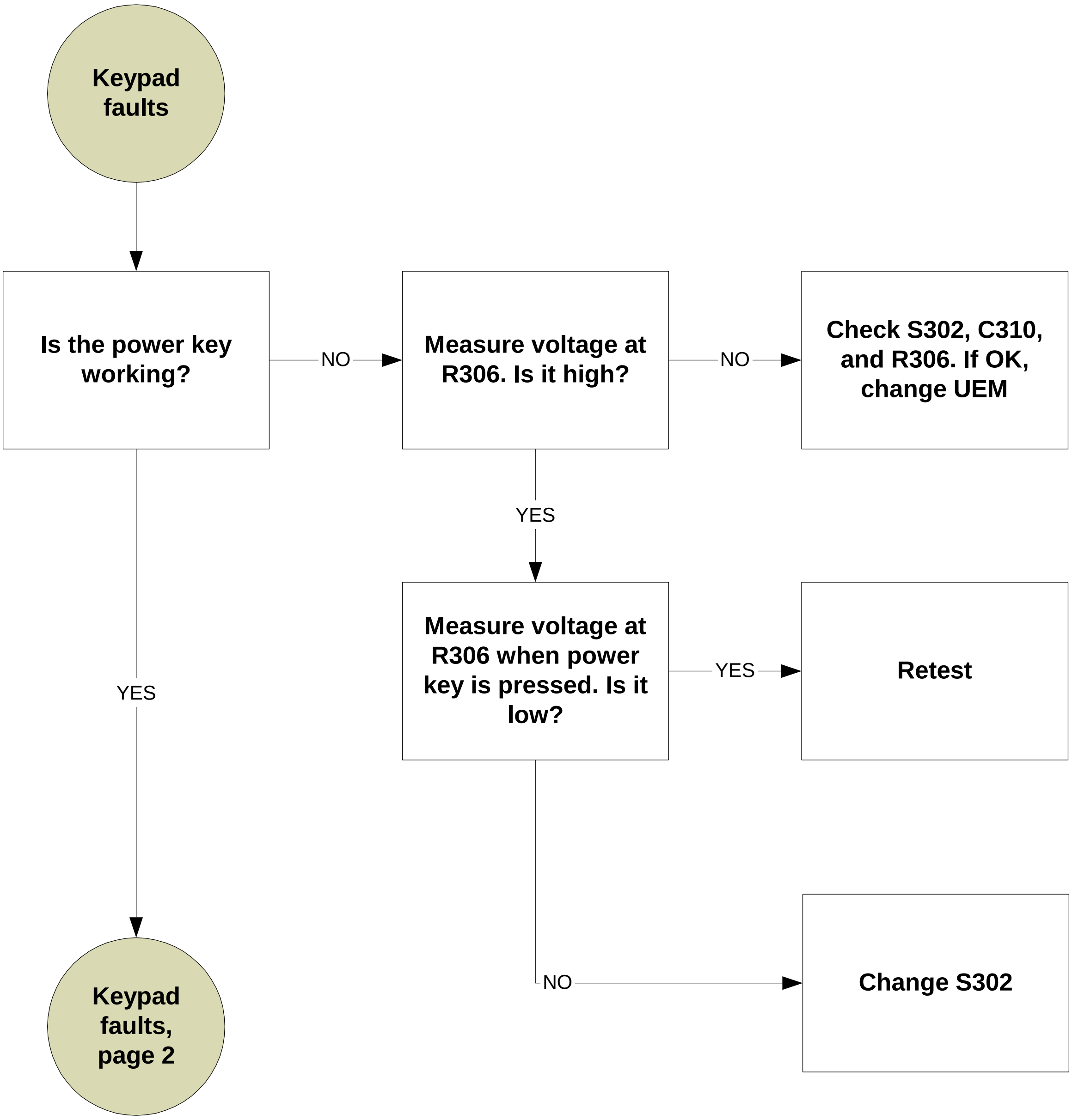
Display faults



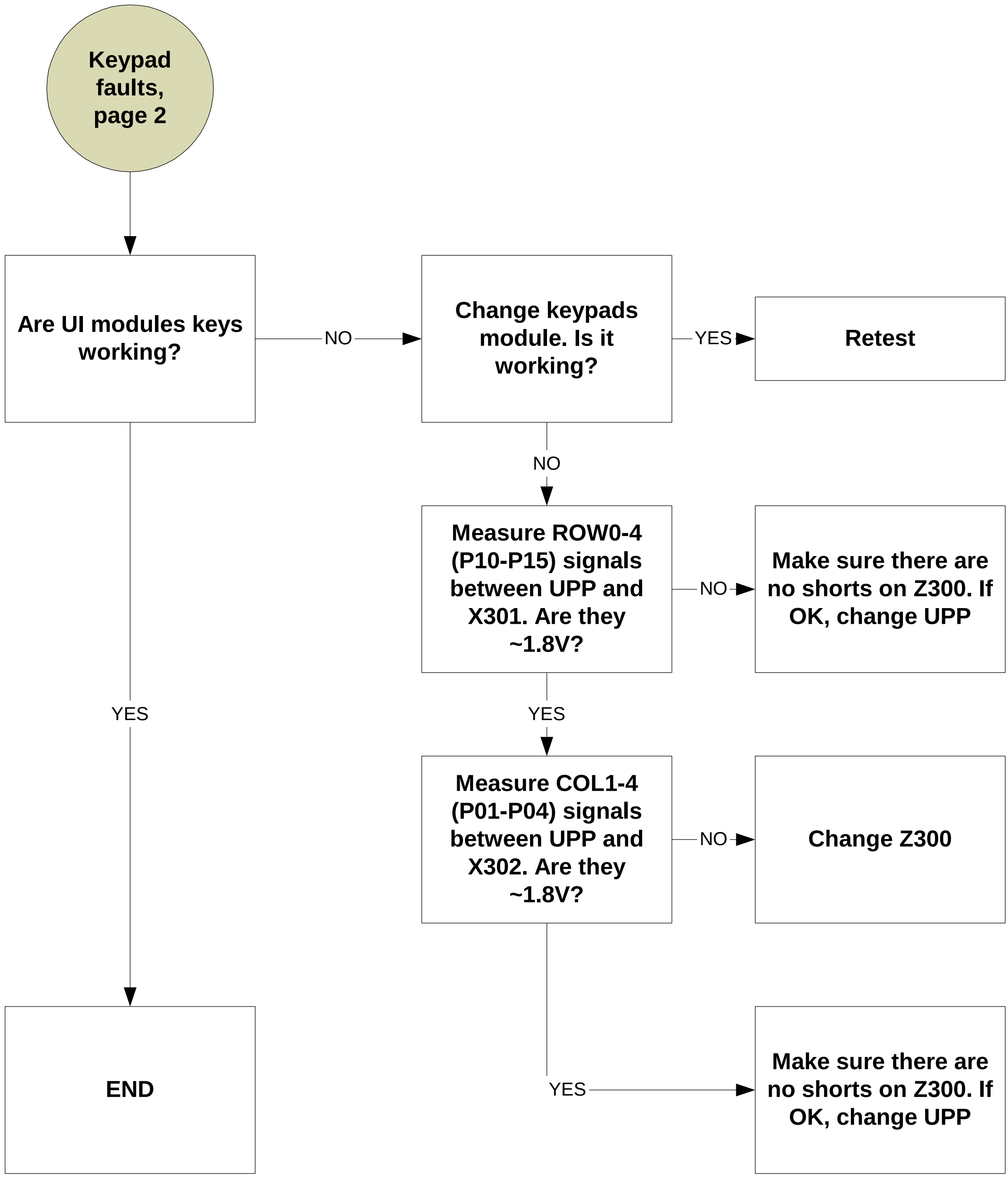

Display faults, page 2
Does the Display start?
NO
Try changing display module. Does it work?
YES
Retest
NO
Set phone in Local Mode. Use Phoenix "Message Sender" and navigate as follows: DEV_HOST-->DEV_PC-->PN_TEST-->OBJ_ROUTING_REQ-->OBJ_PC-->UTID-->TEST_UI_TEST_REQ-->TEST_DISPLAY_SET-->NUM_SB-->TEST_SB_UI_DISPLAY_PATTERN-->SB_LENGTH. Select "TEST_PATTERN_ALTPIXELS" and click "Send"
YES
Check VIO and VFlash1 at X302. Also, check LCD signals LCDCSX (pin5), LCDCLK (pin4), LCDSDA (pin3), and LCDRESX (pin2) at X302. Is signal OK? (Refer to Display section)
NO
Change UPP
YES
Change Display
END

Keypad faults

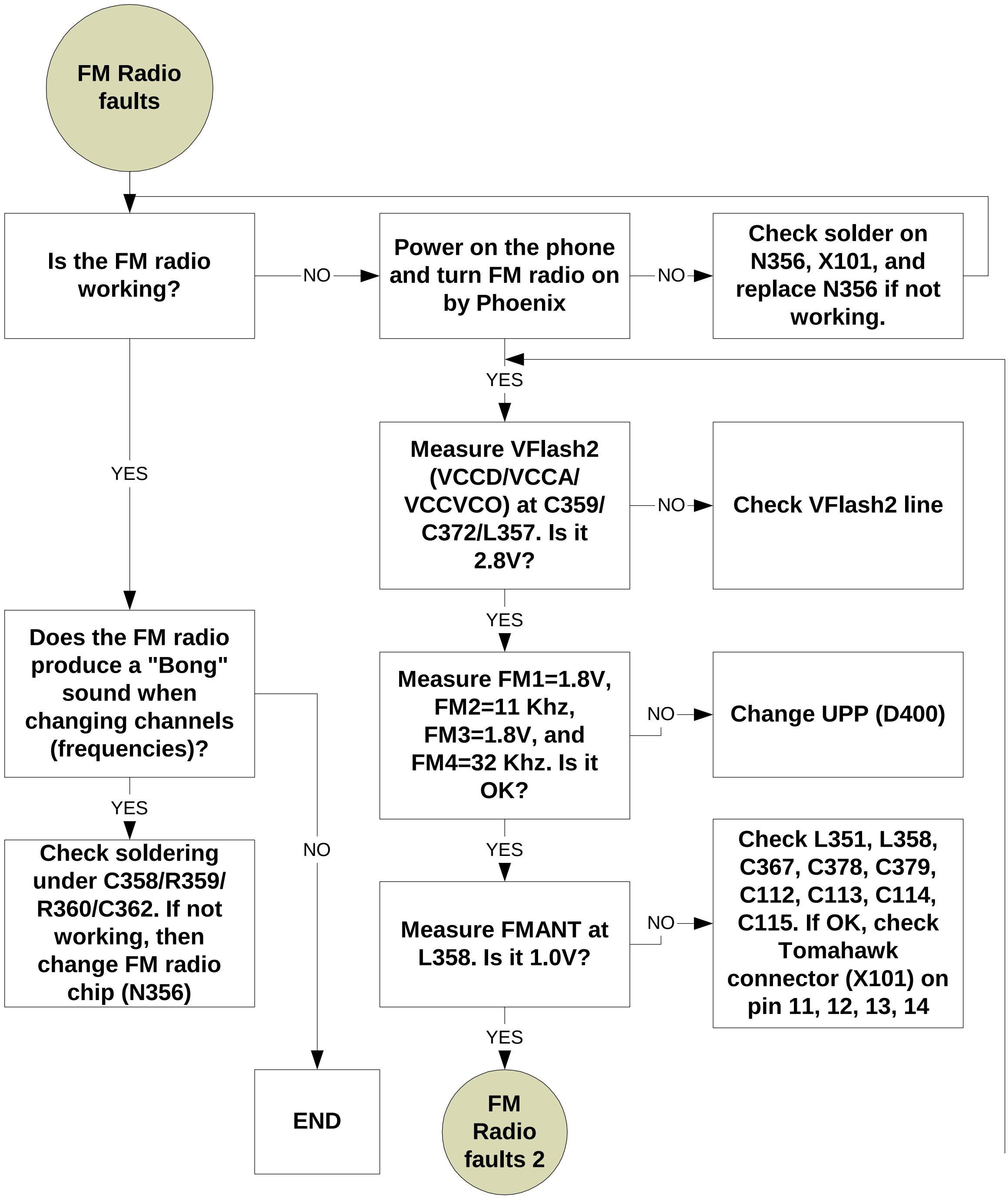
Power key

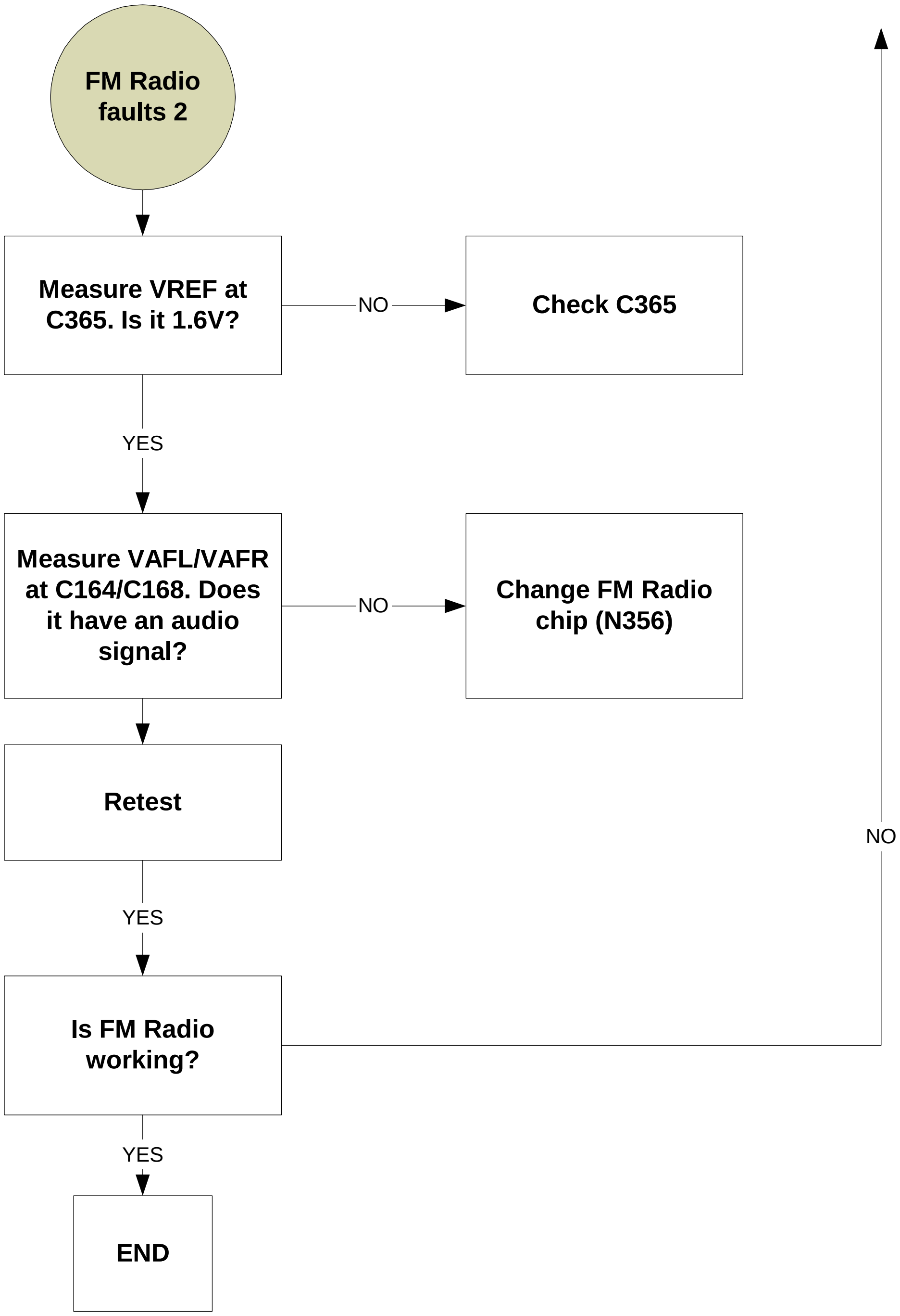


UI modules


Keypad faults, page 2
Are UI modules keys working?
NO
Change keypads module. Is it working?
YES
Retest
NO
Measure ROW0-4 (P10-P15) signals between UPP and X301. Are they ~1.8V?
NO
Make sure there are no shorts on Z300. If OK, change UPP
YES
YES
Measure COL1-4 (P01-P04) signals between UPP and X302. Are they ~1.8V?
NO
Change Z300
END
YES
Make sure there are no shorts on Z300. If OK, change UPP

FM Radio


FM Radio faults
Is the FM radio working?
NO
Power on the phone and turn FM radio on by Phoenix
NO
Check solder on N356, X101, and replace N356 if not working.
YES
Measure VFlash2 (VCCD/VCCA/ VCCVCO) at C359/ C372/L357. Is it 2.8V?
NO
Check VFlash2 line
YES
Does the FM radio produce a "Bong" sound when changing channels (frequencies)?
YES
Measure FM1=1.8V, FM2=11 Khz, FM3=1.8V, and FM4=32 Khz. Is it OK?
NO
Change UPP (D400)
YES
Check soldering under C358/R359/ R360/C362. If not working, then change FM radio chip (N356)
NO
YES
Measure FMANT at L358. Is it 1.0V?
NO
Check L351, L358, C367, C378, C379, C112, C113, C114, C115. If OK, check Tomahawk connector (X101) on pin 11, 12, 13, 14
YES
END
FM Radio faults 2



GPS Module

Overview

The GPS circuitry utilizes RF signals from satellites stationed in geosynchronous orbit to determine longitude and latitude of the handset. The GPS circuitry is completely separate of the CE circuitry and is located almost exclusively on the secondary side of the PWB underneath the display module (see the following figure).

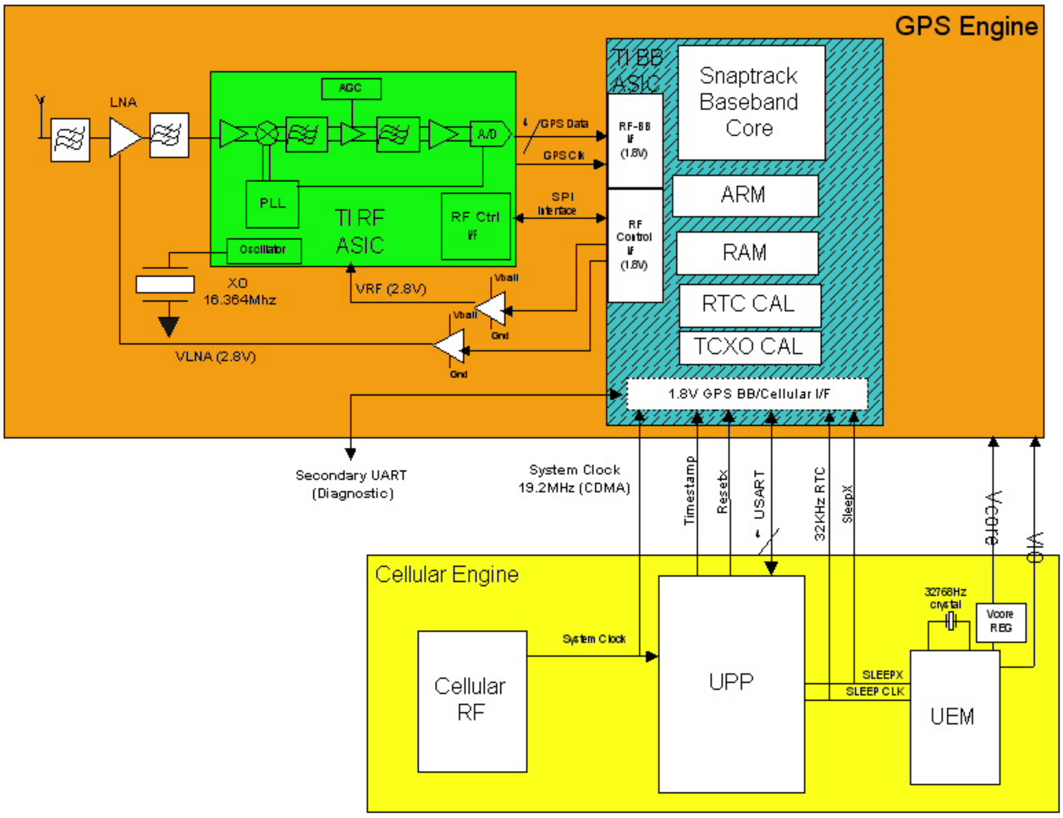


Figure 11: GPS block diagram

The basic GPS BB troubleshooting method is to put the GE and CE in the proper mode, then check to make sure that necessary inputs from the CE are good (power, clock, etc.). Then, ensure that these inputs produce the proper outputs. Because of the large level of integration (most functionality is contained in the two ASIC chips), the amount of diagnostics one is able to do is limited.

Prior to performing diagnostics, perform a visual inspection on the GPS circuitry to see if the problem is physical (dislodged parts, corrosion, poor solder joints, etc.)

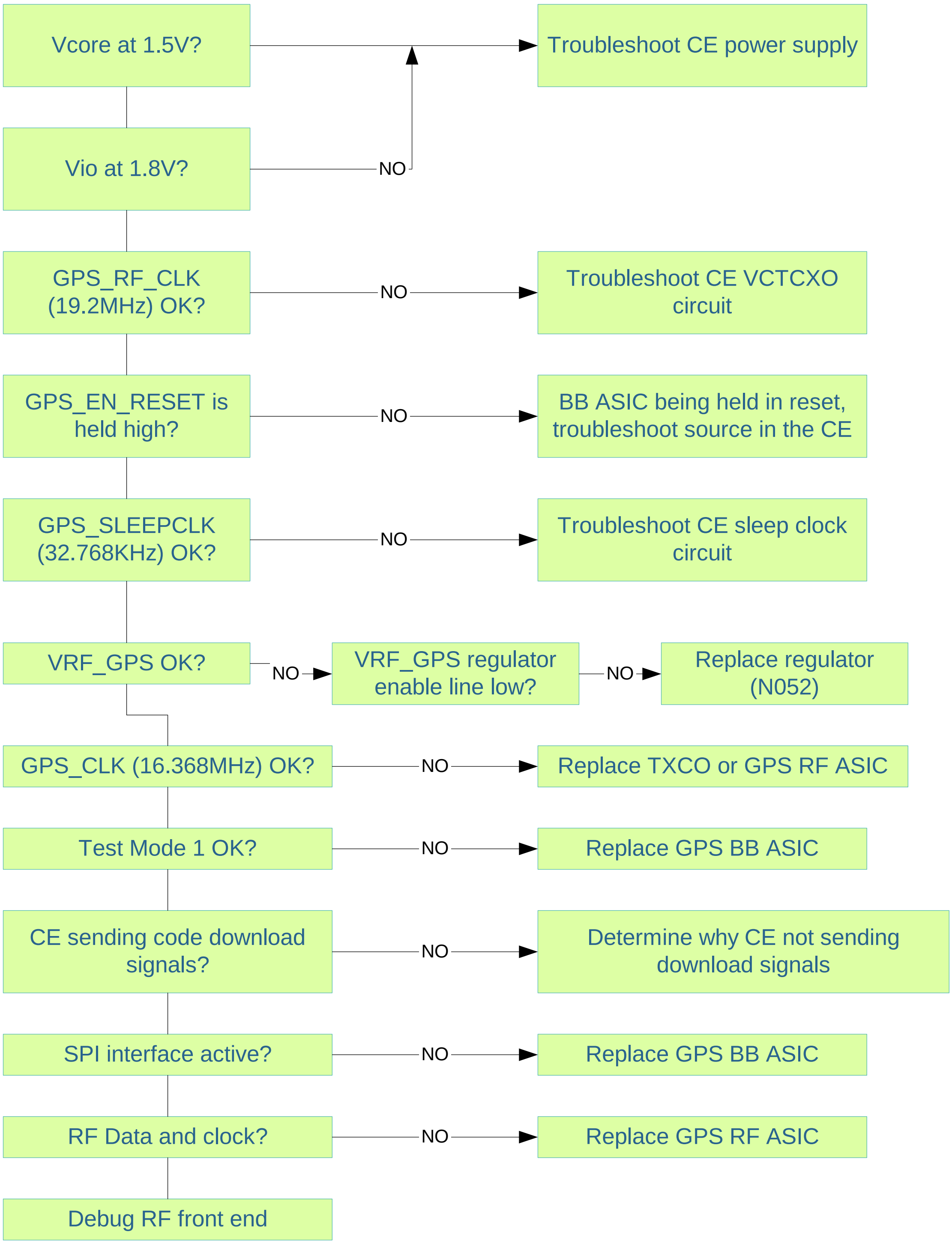


Figure 12: GPS troubleshooting flowchart

